Investigating the Benefit of Silicon Carbide for a Class D Power Stage

Verena Grifone Fuchs1,2, Carsten Wegner1,2, Sebastian Neuser1 and Dietmar Ehrhardt1

1 University of Siegen, Siegen, NRW, D-57068, Germany
verena.grifone@uni-siegen.de

2 CAMCO GmbH, Wenden, NRW, D-57482 Germany
carsten.wegner@camco.de

Abstract

This paper analyzes, in which way silicon carbide transistors improve switching errors and loss associated with the power stage. A silicon carbide power stage and a conventional power stage with super-junction devices are compared in terms of switching behavior. Experimental results of switching transitions, delay times and harmonic distortion as well as a theoretical evaluation are presented. Emending the imperfection of the power stage, silicon carbide transistors bring out high potential for Class D audio amplification.

1. INTRODUCTION

Linearity and efficiency of Class D amplifiers have been improving continuously during the last two decades. Effort was made on optimizing modulator topologies and feedback error correcting loops. The latest progress in semiconductor technology allows emendations by virtue of the switching device. High breakdown voltages combined with low on-resistance and low gate charges bring out high potential for silicon carbide devices in audio amplification.

Aside from the modulation of the input signal into a PWM-signal, also the power stage generates errors.

Switching loss, timing errors and distortion of the output signal are associated with a non-ideal switch. Delay times due to non-linear gate capacitances and blanking times with respect to finite rise and fall times lead to incorrect switching. These timing errors results in noise and distortion on the output signal and demand feedback loops and complex error correction schemes within the modulator.

Improving switch-mode amplifiers, previous work has mainly focused on modulators and feedback loops. This paper will focus on emending the imperfection of the switching devices using silicon carbide for the power stage.

2. THE BENEFIT OF SILICON CARBIDE

The most important characteristic of silicon carbide is the three times wider band-gap compared to conventional silicon and the ten times higher breakdown voltage of the electrical field. Higher temperature capabilities and marginal storage of charge carriers within the semiconductor are further benefits. These properties allow a device with high breakdown voltage, low on resistance and low gate charge at the same time. In this section, the benefits of using a SiC device will be discussed particularly with regard to a class D power stage.

2.1. Higher Breakdown Voltages

Especially in power amplifiers, a high breakdown voltage and a low on resistance is always a trade-off. Silicon carbide devices offer a low on-resistance (<100mΩ) at breakdown voltages up to 1200V compared to equivalent silicon transistors. Decreasing conduction loss will allow higher efficiencies and less cooling.

2.2. Faster Transitions

Low gate charges and small gate capacitances make faster current and voltage transitions possible. Hence, bridge and gate signals are closer to an ideal signal causing less PWM errors and switching loss. Amplifier linearity and efficiency will be improved.
Shorter delay times and a quicker turn-off process permit a smaller dead time for switching the half bridge transistors. Reduced blanking times tend to increase PWM timing and allow higher duty cycle variations. Relating to this, the quality of the audio signal is enhanced. Due to the rapid voltage drop of the bridge voltage, the voltage-time-integral is enlarged, as the correct value is reached earlier. Accordingly, the mean value of the PWM is increased, achieving higher output voltages with the same input signal.

A faster transition from cut-off mode to saturation mode of the transistor also reduces switching loss. If the switching energy is smaller with the same cooling it may occur more often per second and the switching frequency can be increased. A higher switching frequency enlarges the bandwidth of the feedback loop. The benefit is more open loop gain in the audio band and less distortion, when the loop is closed. Operating at the same switching frequency, less cooling would be necessary. Smaller heat sinks reduce case size and costs.

2.3. Enhanced Body Diode

By virtue of the material properties, the silicon carbide body diode has very low reverse recovery charge and a small reverse recovery peak current. In standard applications, the reverse recovery of the body diode triggers resonance in the device capacitance and stray inductance of package and circuit. The high frequency oscillation results in energy loss and electromagnetic interference (EMI). A silicon carbide body diode causes less ringing of the switching signal due to the small reverse recovery charge. The smaller overshoots store less energy, reducing loss and electromagnetic interference [1].

2.4. Higher Operating Temperatures

As the maximum junction temperature of SiC-devices is higher, a larger amount of heat can be dissipated with the same heat sink. Down sizing the heat sink, again, decreases case sizes and costs.

3. MEASUREMENTS

Analyzing the benefit of silicon carbide for class D audio, two power stage prototypes are realized. The silicon carbide prototype comprises the “Z-FET” from Cree (CMF20120D), the conventional power stage is assembled with a “CoolMOS” super-junction device from Infineon (IPW65R080CFD). Both devices are enhancement type field-effect transistors (normally-on MOSFETs). Designed for ±120V, the layout of the PCB (6x-multi layer) is identical for both prototypes. The power stage circuit is illustrated in Figure 1 and differs solely in driving voltage for the power transistors. Both transistors have the same on-resistance $R_{DS}=80\,\text{m}\Omega$ and a comparable current capability ($I_{D,\text{rms}}=25\,\text{A}$). The breakdown voltage is $1200\,\text{V}$ for the Cree and $650\,\text{V}$ for the Infineon device.

Operating at a switching frequency of $400\,\text{kHz}$, the power stage is a half bridge topology with a $4\Omega$-resistive load. Signals above the cut off frequency of $30.5\,\text{kHz}$, are attenuated by a $2^{nd}$ order low-pass filter with $L=18\,\mu\text{H}$ and $C=1.5\,\mu\text{F}$. An iron powder core inductor and a MKP film capacitance is used.

The input signal is a $1\,\text{kHz}$ sine, generated by a DSP (“piccolo”-series from TI). The exact values of a $1\,\text{kHz}$-sine, sampled with $400\,\text{kHz}$, are stored in a look-up table. The amplitude of the stored sine is 1, but can be modified with an attenuation factor. This factor is multiplied with the values in the look-up table within the DSP and will be referred to as “modulation index”. Computing the PWM, a linear interpolation is made between two samples. The calculated switching times are set by a high-resolution PWM module with an accuracy of $16\text{bit}$.

Measurements in section 3.1 to 3.3 are made for an output voltage of $33\,\text{V}$ and a modulation index of $0.8$. During all measurements the dead time for the silicon carbide half bridge is set to $35\,\text{ns}$ and $120\,\text{ns}$ for the conventional devices. The regulated supply voltage for the half bridge is $\pm 50\,\text{V}$.

3.1. Gate Signals

The gate drive circuit is the same for both prototypes, except for the gate-source voltage for turn-on. The floating gate-source-voltage is generated directly on board by a LLC DC/DC converter. Turning on the silicon carbide transistor $V_{G\text{on}}=+20\,\text{V}$ is recommended, the super-junction device is turned on with $+12\,\text{V}$. A voltage regulator adjusts the gate voltage respectively. The turn-off voltage, $V_{G\text{off}}=–4\,\text{V}$, is equal for both devices.

The external gate resistor network, also illustrated in Figure 1, is a parallel connection of a $6.8\,\Omega$-resistor and a diode in series with a $1\,\Omega$-resistor for both prototypes. The values for the internal gate resistance, given in the datasheet, are $R_{G\text{in}}=5\,\Omega$ for the silicon carbide and...
$R_{G,SJ}=0.75\Omega$ for the super-junction device. A more detailed discussion about the devices is given in [2].

![Figure 1: Basic schematic of both power stages](image)

Both transistor pairs are provided with the same gate current for switching. The gate current is monitored for the turn-on and the turn-off event during a switching cycle. Measuring the voltage over the external gate resistors $R_{111}$ and $R_{110}$ of the high side driving circuit, the current is determined.

In Figure 2 and Figure 3, the voltages of the high side resistors ($R_{111}$, $R_{110}$) are plotted for an output voltage of 33V and a modulation index of 0.8. The current values are determined in the statistic beneath the voltage plot, dividing the measured voltage by the resistor value. The statistic displays maximum, minimum and mean value of the current, as well as the standard derivation over 500 cycles.

![Figure 2: Gate current for switching the SiC device](image)

The peak turn-off current is approximately -3.5A (sum of both branches); the peak turn-on current is around +1.6A (for $I_{G,\text{on}} (SJ)$ note cursor value of Channel 1, Figure 3). The waveform shapes are different, as unequal gate capacitances have to be charged and discharged. The following measurements will demonstrate the influence of the capacitances on the switching signals.

### 3.2. Rise and Fall Times

Rise and fall times of the bridge voltage are determined for both prototypes with $m=0.8$. With the same modulation index, the SiC prototype generates a higher output signal. Peak voltages are $V_{\text{out, pk}} (\text{SiC}) = 35V$ and $V_{\text{out, pk}} (SJ) = 33V$ (see 2.2 & 3.4).

The following figures show the 90%-10% transition of a switching cycle triggered at 33V output voltage. Bridge voltage (ch.3/blue), output voltage (ch.2/red) and the gate-source voltage of high- (ch.1/yellow) and low-side (ch.4/green) are displayed. The rise and fall times can be taken from the statistics beneath the voltage plots.

![Figure 3: Gate current of the super-junction device](image)
The SiC power stage requires half the time for the falling transition: $t_r(SiC) = 20.7\,\text{ns}$ vs. $t_r(Si) = 43.2\,\text{ns}$. Also, the transitions of the gate signals are faster, as discussed in section 2.2, p.1. Under the given conditions, the rise time of the bridge voltage is approximately the same for both power stages ($t_i(SiC) = 29.6\,\text{ns}$ and $t_i(Si) = 31.2\,\text{ns}$).

The rising edge of the super-junction half bridge is accelerated by the reverse recovery process of the low-side body diode. Under positive load current, the high-side device determines the rising transition. Prior to the bridge voltage slope, the load current commutates from the low-side body diode into the high-side FET [3]. When the FET enters saturation region, the commutation process is completed and reverse recovery of the diode starts. Running to the negative supply, the reverse recovery current holds the bridge voltage down (see Figure 5). During the entire time, the reverse recovery current stores energy in the parasitic inductances. Once the reverse recovery is completed, the current commutates into the output capacitances of the transistors. Due to the high current, the capacitances are rapidly charged, provoking the high $du/dt$ of the rising edge. As reverse recovery charge of the SiC device 7 times lower, the transition is not accelerated in the same way.

In Figure 5 the bridge voltage (of the super-junction device) starts to rise, as soon as the gate-source voltage of the high-side FET exceeds threshold voltage. As the reverse recovery process starts, the bridge voltage is clamped and shows an oscillation. After reverse recovery is completed, the voltage transition occurs with a steep slope. Figure 4 illustrates, that the reverse recovery time is much shorter and the voltage slope is less. The enlarged illustration of the rising edge in Figure 6 and Figure 7 clearly display the impact of reverse recovery on the transition.

The falling edge of the SiC half bridge is accelerated by hard switching. In consequence of the fast gate signals and the short dead time, the low-side gate signal ascends before the transitions completes. Hence, the low-side transistor turns on while the bridge voltage falls, conducting almost during the entire off-time. In contrast to that, the super-junction device is soft switching. By reason of the large delay time, the low-side signal ascends after the voltage transition. During the delay time, the current commutates from the high-side FET into the low-side body diode. Thus, the turn-on process of the low-side device is a zero voltage switching transition (ZVS) and the falling edge is not accelerated.

In Figure 4, the low-side gate voltage of the SiC device ascends at about 10% of the bridge voltage drop. Rising fast, the peak driver voltage is reached after 100ns. Figure 5 shows, that the low-side signal does not reach the peak driver voltage during the off-time. The device turns on for a short interval of approximately 80ns.

### 3.3. Delay of the Bridge Voltage Transition

The delay time is measured from the initiation by the gate driver to the zero crossing of the bridge voltage (half transition). Again, the high-side switching cycle is triggered at an output voltage of 33V with $m=0.8$. Active switching is monitored for both prototypes. The initiation the switching event is displayed by the output voltage of the gate driver with respect to the source pin. Figure 6 - Figure 9 illustrate the driver voltage (ch.4/ green), the gate-source voltage (ch.1/yellow), the bridge voltage (ch.3/blue) and the output voltage (ch.2/red).
Comparing the delay times, the influence of the gate capacitances becomes evident. Turn-on delay is smaller by a factor of 2.5 ($t_{\text{d,r(SiC)}} = 41.6\,\text{ns} / t_{\text{d,r(SJ)}} = 78.6\,\text{ns}$), and turn-off delay is shortened by half ($t_{\text{d,f(SiC)}} = 38.2\,\text{ns} / t_{\text{d,f(SJ)}} = 94.2\,\text{ns}$). Also the effect of reverse recovery is evident at the rising edge, as discussed in Section 3.2. During a switching cycle, the capacitances $C_{\text{gd}}$, $C_{\text{gs}}$, and $C_{\text{ds}}$ are charged and discharged, where the major contribution is $C_{\text{gs}}$. The total gate charge of the conventional transistor is almost twice as high ($Q_{\text{g(SJ)}}=170\,\text{nC} \text{ vs. } Q_{\text{g(SiC)}}=90\,\text{nC}$). Especially due to the low gate-drain component, the gate voltage of the SiC device almost follows the driver output, whereas the silicon device has to transcend the miller plateau. A more detailed analysis of the gate capacitances relating to the turn-off event is made in [2].
Shorter delay times and faster transitions reduce blanking times and allow higher duty cycle variations, as seen in the next section.

3.4. Switching Cycle at 95% Modulation

The following measurement shall illustrate the benefit of the silicon carbide power stage having faster transitions and the shorter delay times. Both prototypes are driven with the same modulation index of 0.95, but different output voltages are achieved. In order to show the difference in duty cycle variation, the switching cycle is triggered at the maximum output voltage. The following figures display output voltage (ch.2/red), bridge voltage (ch.3/blue) and gate-source signals (high-side ch.1/yellow, low-side ch.4/green).

![Image](Figure 10: Maximum duty cycle transitions at m=0.95 for the SiC power stage)

The peak output voltage of the SiC power stage is 2.5V higher for the same modulation index: $V_{\text{out pk (SiC)}} = 43.6V$ vs. $V_{\text{out pk (SJ)}} = 41.2V$. The faster transitions enlarge the voltage time integral and decrease switching loss. Thus, the mean value of the PWM rises and the output voltage is higher (Section 2.2, p.1).

At higher output voltages, the minimum off-time of the bridge signal is smaller. The off-time in displayed in the SiC-plot (120ns) is approximately 100ns shorter compared to the super-junction-plot (220ns). However, the low-side gate signal rises to the peak driver voltage of 20V turning on the low-side FET. The gate-signal of the super-junction device stays zero, as the dead time is longer and the high-side gate voltage is still decreasing. Hence, the body diode is conducting during the entire off-time and conduction loss is enlarged.

The enhanced switching signals also emend THD: for $m=0.95$ the THD of the SiC power stage is 0.5% in contrast to 1.7% for the super-junction half bridge. A detailed study is made in the next section.

It is worth mentioning that the dead time of the conventional power stage is as long as the off-time of the SiC-switching cycle. Thus, higher duty cycle variations with accurate gate signal transitions are possible, using silicon carbide switching devices.

3.5. THD + N and FFT Analysis

Audio performance and linearity is investigated, comparing the total harmonic distortion and the FFT analysis for a particular input signal.

All measurements are performed with the Audio Precision AP2700 audio analyzer and an Aux25 low-pass filter. Both prototypes are supplied with the same regulated, constant DC voltage, indicating only minimal voltage ripple to the power stage. Thus, power supply perturbations can be neglected.

Figure 12 illustrates total harmonic distortion plus noise over the effective output voltage for the Silicon (blue) and the SiC half bridge (pink). The input signal is a 1kHz sine with a logarithmic amplitude sweep from modulation index 0 to 1. The maximum effective output voltage at $m=1$ is 27V for the silicon and 30V for the SiC power stage.

![Image](Figure 11: Maximum duty cycle transitions at m=0.95 for the super-junction power stage)
At low output voltages, the noise floor dominates the curve, having a slope of -20dB/dec. Reading above 1.5V, harmonic distortion becomes eminent. The distortion of the SiC power stage remains at lowest values almost up to the maximum output voltage. At a modulation index of 0.98 the THD equals still 0.55%, at m=1 the THD is 0.76. The super-junction power stage reaches clipping much earlier, at m=0.8 the THD equals 1.18%, at m=1 the THD is 1.98%.

Reading below 7.5V output voltage, the THD of both power stages is comparable. Lowest level is around 0.4%, predominantly determined by the DSP. Towards higher output voltages the SiC power stage has a remarkable better THD. Distortion is emended by the enhanced switching signals and the significant lower dead time. The enhanced switching signals (faster transitions, less delay times, higher duty cycle variation as described before) reduce PWM errors especially at higher modulation indices. Dead time has a significant contribution to THD, when the load current exceeds the ripple current [4]. With a ripple current of 3.47A peak to peak, the effective output voltage, where dead time becomes eminent, calculates to 5V. The influence of the dead time can be observed at output voltages around 7.5V, where the THD curves intersect.

As an addition to the THD+N plot, a FFT analysis and the equivalent components in the time domain are given. The FFT analysis is made at 1/8 of the maximum output power, which is 9.82V for the silicon and 10.78V for the SiC power stage. (1/8 power represents the average power of an audio signal driven to occasional clipping.)

The FFT analysis for the super-junction power stage indicates, that the uneven harmonics, especially k5, are slightly damped. In the spectrum of the SiC half bridge, the k2-component is smaller.

Figure 13 and Figure 14 show the THD+N spectrum for 1kHz at a modulation index of m=0.339 for the SiC half bridge (pink) and m=0.358 for the super-junction power stage (blue, lower chart). The indicated THD+N values according to these modulation indices are approximately the same: THD+N_SiC=0.43% (47.26dB) and THD+N_SJ=0.45% (46.93dB).

The FFT analysis of THD+N components for the output power for the SiC-power stage (THD+N=0.43)

The FFT analysis of THD+N components at 1/8 super-junction power stage at 1/8 output power. (THD+N=0.45)

The FFT analysis for the super-junction power stage indicates, that the uneven harmonics, especially k5, are slightly damped. In the spectrum of the SiC half bridge, the k2-component is smaller.

Figure 15 and Figure 16 illustrate the voltage of the THD+N components. The output signal of the power stage is displayed in red (ch.2), the associated components without the fundamental in blue (ch.3).
 Remarkable lower delays (factor 2.5) and faster transitions with less reverse recovery impact result in higher output voltages and larger duty cycle variations for the SiC power stage. Reduced blanking times permit a significantly shorter dead time for the SiC half bridge (factor 3.4), emending the measured THD. Especially towards higher output voltages, the THD+N curve remains constant at lowest level without complex optimization. At a modulation index of 0.98 the THD equals 0.55%, at m=1 the THD is 0.76. Lowest values are around 0.4%.

Faster voltage transitions and minor reverse recovery contribution will also improve efficiency. An investigation of switching and conduction loss is part of the ongoing work.

The emendation in terms of switching behavior is also applicable to full bridge configuration. Improvements concerning EMI and loss are achievable using silicon carbide devices. Hence, theoretical and experimental evaluation concerning THD, efficiency and EMI will be made, further investigating the benefit of silicon carbide.

5. ACKNOWLEDGEMENTS

This work was supported by CAMCO Produktions- und Vertriebs-GmbH für Beschallungs- und Beleuchtungsanlagen, Cree Inc. and Infineon Technologies. The author would like to thank Cree Inc. and Infineon for providing samples. Thanks to the team at CAMCO for the kind assistance and for sharing measurement equipment.

REFERENCES


