Variability Aware Design in nm Era

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As the technology scales, process, voltage, and temperature, variations (PVT) and model inaccuracies impact design yield. In this talk, a predictive analytical technique based on statistical analysis methodology targeting both memory and custom logic design applications is highlighted. The methodology hinges on Mixture Important Sampling (MIS) is 5-6 orders of magnitude faster than Monte Carlo and a few orders compared to recent techniques. For advanced technologies, we extend the methodology to enable key features such as the Front End of the Line (FEOL) and back end of the line (BEOL) parasitic extraction and TCAD for manufacturability for 16nm and below. This increases the statistical confidence in the functionality and operability of the system-on-chip as a whole. The methodology is further extended to predict aging effects in memories and the utility of this technique is demonstrated through hardware fabrication.

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