**Chair of Analogue Circuits and Image Sensors**
**Universität Siegen**

## Circuits and Sensors Seminar

# Designing with emerging reconfigurable nano-technology

Prof. Akash Kumar, TU Dresden

***When:*** 2PM, Thursday the 5th of November, 2020
***Where:*** Online, Joining Instructions below
https://uni-siegen.zoom.us/j/96677401186

Meeting ID: 966 7740 1186
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*Abstract*

Application Specific Integrated Circuits (ASICs) based on CMOS technology have been the workhorse of electronic engineers as they boasts of a circuit suited for a "specific" purpose with high performance to area ratio. This static design of CMOS technology is simple to build and is applicable to a wide range of application scenarios. However, with Moore's law offering limited cost and performance gains with newer technology nodes, researchers are looking for beyond-CMOS technologies.

Silicon nanowire based functionality enhanced transistors also called reconfigurable transistors (RFETs) provide an alternative path to increase the number of functions offered by a particular logic gate. Reconfigurability in SiNW RFETs allows the freedom of choosing symmetrical p-type or n-type functionality from the same device as programmed at runtime through a dedicated program voltage. In this talk, I will provide an overview into the devices, followed by our work in logic and physical synthesis flows for supporting such reconfigurable transistors. Lastly, I will provide an insight into how such reconfigurable devices can be an ideal candidate for designing inherently secure circuits.

*Speaker Bio*

Akash Kumar is a chaired Professor of Processor Design (with tenure) in the department of Computer Science at Technische Universität Dresden (TUD), Germany. From 2009 to 2015, he was with the Department of Electrical and Computer Engineering, NUS. He received the joint Ph.D. degree in electrical engineering in embedded systems from Eindhoven University of Technology (TU/e) and National University of Singapore (NUS), in 2009; joint Master's degree from TU/e and NUS in 2005 in embedded systems and Bachelor of Computer Engineering degree from NUS in 2002. His research interests span various aspects of design automation in the context of embedded real-time systems with particular emphasis on reliable, resource-efficient and predictable architectures for embedded systems, including FPGA-based architectures. He has received Best Paper Award at DATA 2018, and best paper award nominations at DATE 2015, 2017 and 2020, FPL 2014, GLSVLSI 2014, ISVLSI 2020 and Supercomputing Conference 2015. His group also received HiPEAC Technology transfer award 2019.

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