Abstract

The size of integrated circuit (IC) die has continuously increased due to Moore's law in the last few decades. A large system on chip (SOC) contains many complex analog and digital blocks which must run at high clock rate to support the needs of today's applications. These large SOCs suffer from global interconnect delay bottleneck and increased design complexity. In order to deal with this problem, the SOC can be divided into smaller chips which could be placed together in a multi-chip-module (MCM) or in a 2.5D interposer system. The chips must communicate with each other, which poses the challenges of transmitter and channel design along with system optimization.

This work addresses the three challenges of multi-chip system design: (*i*) transmitter design for moderate speed unterminated signalling and high speed multi-Gb/s terminated signalling, (*ii*) channel analysis and design for minimum area usage while meeting the bandwidth and energy requirements of memory and high speed interfaces, (*iii*) design methodologies for transmitter and channel co-design, and design flow for optimum memory interface in multi-chip systems.

This work tackles the transmitter design challenge for multi-chip systems by offering two types of transmitters: an unterminated low swing driver for moderate data rates, and a high speed terminated transmitter for multi-Gb/s communication interfaces. Both transmitters are designed in 22 nm FDSOI technology and taped out. Channel analysis is done for various width, spacing and length of interconnects in 2.5D silicon interposer technology. The signal integrity analysis of memory and serial interfaces (SERDES) directs the designer to choose the right width and spacing of channel for optimum energy or area metrics. Two design methdologies are presented in this work: first is current mode logic (CML) differential driver and interposer co-design for minimum energy and area performance metric, second is a design flow for optimum memory interface design by choosing the right memory and integration technology based on given cost and bandwidth constraints. The proposed transmitters, channel analysis and suggested methodologies can be used by industry and research community to design energy and area efficient multi-chip interfaces.