Active Thermal Protection and Lifetime Extension in 3L-NPC-Inverter in the Low Modulation Range

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***Abstract*—The switches of multilevel inverters in high-power applications are mounted on dedicated heatsinks and there is no heat sharing among the devices. If one semiconductor device is exposed to excessive thermal stress, then the lifespan of the affected device is reduced significantly. This thermal overload may arise due to degradation of the cooling system, failures in firing or in the drivers, inappropriate placing of the semiconductor devices etc. In this paper, a control scheme is devised that can reduce the thermal stress of a particular semiconductor device; the benefit is that the reduction of the lifetime of this device is avoided. Thus, after detecting of the occurrence of a local thermal overload by temperature sensing on the particular heatsink, the control scheme modifies the pulse width modulation in such a way, that the power losses of the stressed device are redistributed among the other semiconductors without limitations of the inverter current. In previous works, this method was already presented for the higher modulation index range; it is now extended to the low modulation range and is validated by experiments.**

Keywords—Pulse width modulation converter, semiconductor device reliability.

I. INTRODUCTION

In high-power converters the switches are often mounted on dedicated heatsinks, therefore a uniform distribution of the heat among the switches is not always provided. If one semiconductor device (Diode or IGBT) is exposed to excessive thermal stress, a local increase of the temperature occurs that affects significantly the lifespan of the power device. This thermal overload during the operation of a converter may arise due to degradation of the cooling system, failures in firing or in the drivers, inappropriate placing of the semiconductor devices etc. In this following, a control scheme is devised that can reduce the thermal stress of a particular semiconductor device by redistribution the losses in the converter to the other devices that are not affected by the failure. Obviously, if the excessive increase of the temperature is avoided, the reduction of the lifetime of this device is prevented.

The proposed strategy assumes that the temperature of each heatsinks is monitored, thus the occurrence of a local thermal overload can be detected. In such a case, the control changes of the PWM (pulse width modulation) aiming a reduction of the losses in the overheated device and a redistribution of the losses among the other semiconductors that still have an efficient cooling. The modified PWM should have a minimum impact on the operation of the inverter, without limitations or distortions of the inverter current or increase of the ripple of the voltage of the neutral point of the dc-link.

The control scheme proposed in this paper is explained for a Three-level Neutral Point Clamped Voltage Source Converter (3L-NPC VSC) [1], but it is also applicable for any kind of multi-level inverter. Like other control methods that deal with similar issues; it takes advantage of the redundant space voltage vectors to actively redistribute the losses from the overloaded devices to the other cooler semiconductors without using any additional hardware. A main feature of the proposed control strategy is that as a long-term effect the expected lifetime of the power semiconductors is significantly extended because the devices are protected against excessive thermal stress [2]. Therefore this strategy was named **ALE** (active lifetime extension).

Several control methods that aim at the uniform distribution of the load among the semiconductors in the inverter are well-known. The objective of the proposals in [3][4][5] is an homogeneous distribution of the losses under normal operation of the inverter. For this purpose, the topology of the inverter is modified by adding IGBTs parallel to the neutral point diodes to generate additional redundant states of switching states 0 (connection of one of the output phases to the neutral point). The extra states allow the desired uniform relocation of the losses.

In [6] a different approach is presented in which the redundancies of the zero voltage vectors are also utilized for the redistribution of losses. The method is restricted in the low modulation index range for operation with a load of reactive current. In the present work, not only the zero voltage vectors but all the redundancies of space voltage vectors are used. The method can be applied for the whole voltage and current range of the inverter.

In the present work the concept ALE will be realized with space vector modulation. The desired voltage vector is realized by using the three nearest vectors (TNVs); those form the vertices of the triangle, in which the reference voltage vector resides at the moment of sampling. In the high modulation index range, the switching states of any TNVs consist of *redundant* and of *non-redundant* ones. In contrast to this, in the low modulation index range all the switching states of TNVs are *redundant*. Due to the different configurations of the switching states of the TNVs in the different ranges of modulation index, the ALE procedure has to be analyzed in two different steps. In

previous works [7][8] the operation of the inverter in the range of higher voltage when using ALE control strategy was thoroughly examined.

Now the investigation is completed for the operation of the inverter in the range of lower modulation index and the theoretical consideration is validated by experiments.

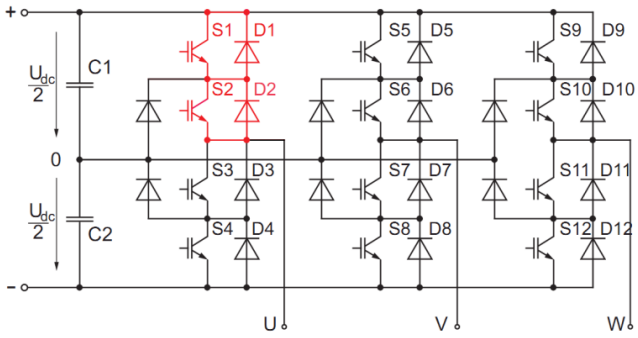

Figure 1. 3L-NPC VSC, in red the devices with higher thermal load

II. STRATEGY FOR LOSS REDISTRIBUTION IN 3L-NPC INVERTER WITH SPACE VECTOR MODULATION IN THE LOW MODULATION RANGE

The modulation index is defined as:

$$m = \frac{U_{LL,1}}{U_{dc}/\sqrt{2}}, \tag{1}$$

Where $U_{LL,1}$ is the rms value of the fundamental of the line-to-line voltage at the output terminals of the inverter and U_{dc} is the dc-link voltage.

To simplify the analysis, it is sufficient to consider the upper leg of phase U of the inverter, depicted with red color in Fig. 1, as the stressed device, in which the thermal load has to be reduced. As already explained, the development of the control method depends upon the value of the modulation index. In the following, only the operation of the inverter in the lower modulation range $0 < m \leq 0.5$ is treated (blue region in Fig. 2), whereas the range $0.5 < m \leq 1$ is explained in [7][8].

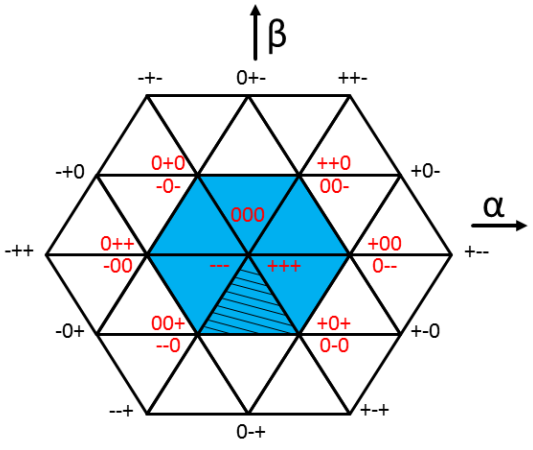

Figure 2. Space vector diagram for a three-level inverter with the redundant states

Fig. 2 shows the space vector diagram of a three-level inverter in the α-β frame of coordinates with the 27 possible switching states. The notation *+/0/-* means that a given phase is connected to the positive dc bus, to the neutral point or to the negative dc bus, respectively. The switching states depicted in red are redundant; they present the same line-to-line output voltage but they are different from each other in terms of common mode voltage and of loss distribution among the switches of the inverter. Hence, the redundant switching states can be used to reduce the common mode voltage, to control the neutral point voltage or to relocate the heat from the stressed switching device.

As mentioned above, the proposed ALE strategy is realized by means of space vector modulation (SV-PWM). There are two ways to implement the SV-PWM: continuous or discontinuous schemes [9]. The continuous PWM (C-PWM) provides better harmonic performance as compared with the discontinuous PWM (D-PWM) but at the cost of higher losses. The continuous PWM scheme is widely used in practical applications. If the thermal overload occurs in one switching device, the active thermal protection mechanism will be operated in the two steps mode. At the first step, the continuous PWM scheme will be changed into discontinuous PWM to reduce the losses of the inverter, in this way the reduction of losses can be achieved with a minimal impact on the system performance. If this action is still not sufficient to keep the stressed device under the thermal limit, the discontinuous PWM will be changed into ALE control scheme to further reduce the losses on the stressed device. Therefore, throughout the paper from the discontinuous PWM (D-PWM) will be used as reference method to compare with the ALE strategy.

A. Relocating losses by using redundant states of space vector modulation in the low modulation range

To illustrate the idea of the proposed concept, it is assumed that the reference voltage vector is located inside of the hatched blue triangle in Fig. 2. The analysis can be carried out in a similar manner for all other blue triangles in the low modulation index range. The switching vectors corresponding to the vertices of the hatched triangle are shown in Fig. 3. These switching vectors are stored in a matrix and arranged in relation to common mode voltage, from low to high, from the left to the right, i.e. the switching vector with the highest positive common mode voltage is located on the right side of the matrix and vice versa. In this arrangement the transition from one switching state to an adjacent one demands only one switching action.

In the normal discontinuous PWM scheme, a set of *three adjacent* vectors is chosen from this matrix to build the inverter voltage corresponding the reference value. The set of three vectors with highest common mode voltage (on the right hand side of the matrix) and the set with lowest common mode voltage (on the left) must be used alternating to stabilize the neutral point voltage of the dc-link in a dedicated control loop that is realized according to [10].

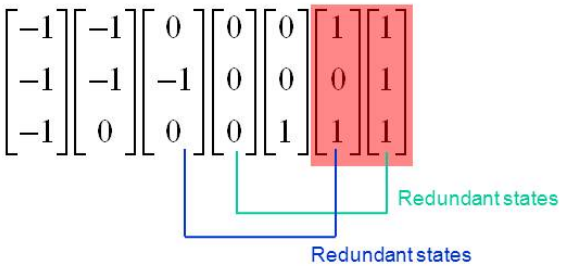

Figure 3. Choice of appropriate switching states

In the case that the ALE strategy is applied for reducing the losses on the upper leg of phase U; all the switching vectors, in which the upper leg of phase U is utilized (e.g. the 2 vectors in red in Fig. 3), will be removed from the calculation. Hence, the output voltage vector must be synthesized by using the remaining redundant states [2]. Yet this exclusion has a negative impact on the control of neutral point because, as it will be explained in the next section, one of the sets of states that are used for the stabilization of the voltage of the neutral point of the inverter is excluded in the modulation.

B. Analysis of the impact of the ALE on the voltage of the neutral point of the dc-link

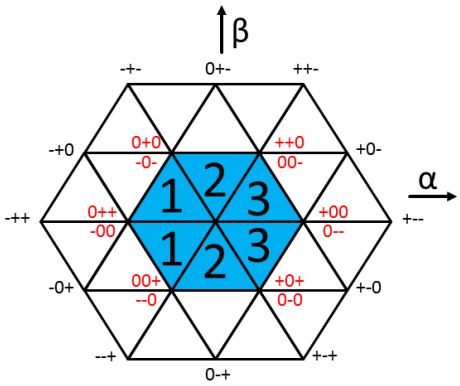

Figure 4. Exclusion of inappropriate switching vectors for reducing the losses of the upper leg of phase U

The ALE strategy can be applied in the whole low modulation index range. Yet its impact on the performance of the neutral point depends on how many switching vectors are excluded from the calculation. Moreover, the number of switching vectors that are allowed for the modulation depends on the location of the reference voltage vector in the α-β-plane. Fig. 4 shows the numbers of switching vectors to be removed from the calculation for reducing the thermal stress in the upper leg of phase U for each of the inner triangles in which the reference voltage vector can be located. For a voltage vector located in the upper or in the lower triangle two states are excluded. For the blue triangles on the right hand side three states are forbidden and for those in the left hand side just one.

Actually, the upper leg of phase U can be completely excluded from the calculation and so its losses can be significantly reduced. Such operation is possible but it causes an excessive ripple on the neutral point and has a negative effect on the system performance and is not considered in the control scheme. Moreover, a tradeoff between the reduction of losses by using the ALE strategy and the increase of the ripple of the voltage neutral point must be achieved by using an operational map.

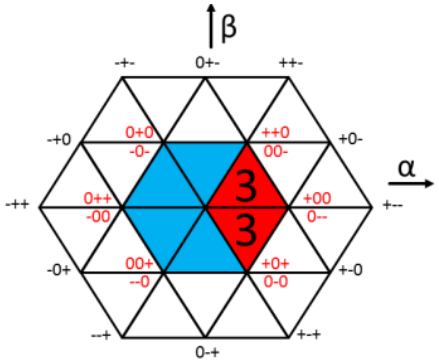

Figure 5. Operational map type A, the red region is dedicated to ALE, the blue one is dedicated to the normal D-PWM

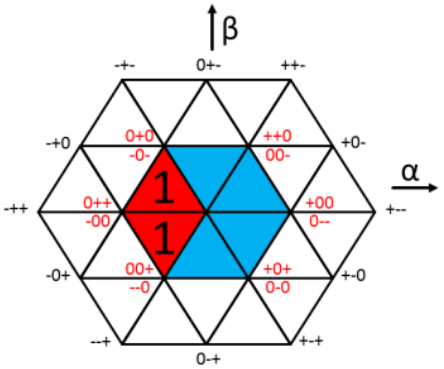

Figure 6. Operational map type B, the red region is dedicated to ALE, the blue one is dedicated to the normal D-PWM

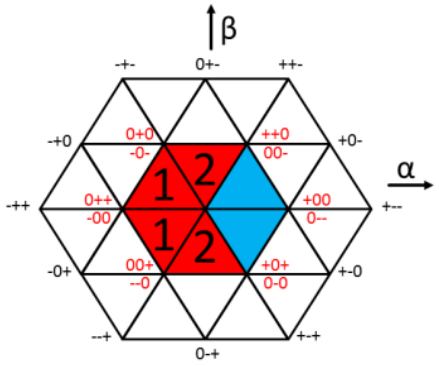

Figure 7. Operational map type C, the red region is dedicated to ALE, the blue region is dedicated to the normal D-PWM

Fig. 5 shows a possible operational map. If the reference voltage vector at the sampling time is located in the red areas and a thermal overload in the upper leg of phase U is detected, the PWM is changed to the modified ALE operation. As explained above, under these conditions three switching vectors must be removed from the calculation and the other redundant switching vectors are used instead of the excluded ones. As long as the reference voltage vector is inside of the red areas,

the upper leg of phase U does not participate in the modulation, its conduction and switching losses are therefore reduced. When the reference voltage vector leaves the red area and enters the blue region, the system returns to normal D-PWM operation and no switching vectors will be removed from the calculation.

In a similar way, the analysis is extended to the operational map of type B in Fig. 6, in which only one switching vector is excluded from the modulation. This mode of operation is expected to result into a smaller ripple of the voltage of the neutral point as in the case of an operation with the map of type A.

The operational map of type C in Fig. 7 is a further extension, where one or two switching vectors are excluded. Of course all three different solutions have a different performance in terms of temperature reduction of the affected device and of the ripple of the voltage of the neutral point. The system behavior for the aforementioned modes or operation was examined in the lab and the results of the measurements are presented in the following.

III. EXPERIMENTAL RESULTS

A. Experimental setup

Figure 8. Heatsinks of the set-up with the 3L-NPC VSI

For the experimental verification of the proposed modulation strategy a laboratory set-up was especially designed. The whole digital control including space vector modulation and field oriented control is implemented by using a single DSP (TMS320F28335). The power part is a three level neutral point clamped converter (3L-NPC), it has a nominal power of 20 kW and feeds a 15 kW standard induction machine. The inverter has 18 dedicated heatsinks, i.e. six heatsinks per phase. The heat-sinks are vertically arranged as shown in Fig. 8. Each one is equipped with a temperature sensor Pt1000 so that the distribution of the temperature the inverter as indicator of the power losses of the IGBTs can be measured. In order to reduce the thermal coupling, each heatsink is covered with a small plastic plate to avoid the air circulation among the heatsinks. The measurement of the temperature of each IGBT takes place after reaching the thermal steady state of the whole system, in which no increase of temperature can be registered. In the steady state the over-temperature are directly proportional to total losses of each semiconductor device [8].

The IGBTs utilized in the downsized laboratory set-up have characteristics for optimized conduction losses; therefore they are intended to replicate in a suitable way the thermal behavior of the high power IGBTs. The rated current of the inverter is of 50 A. The DC link U_{dc} = 350V, the DC capacitor C_{dc} = 4,4 mF and the switching frequency is 5 kHz.

B. Experimental results

The experimental results were obtained for a modulation index m = 0.45, a stator current I = 0.6 $I_{inverter,\ rated}$, a dc-link voltage U_{dc} = 350V and a switching frequency of 5 kHz.

1) Firing pulses of IGBT 1 of upper leg of phase U (the numbering of the switches is given in Fig. 1)

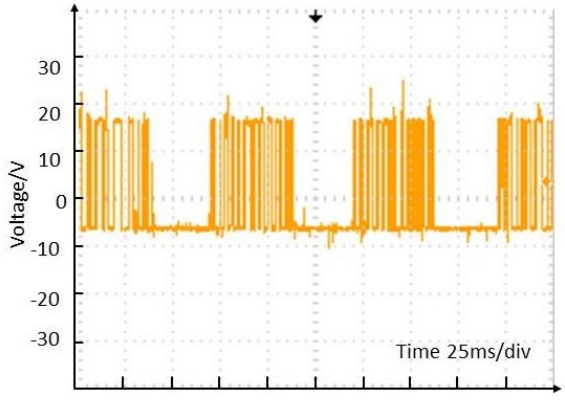

Figure 9. Firing pulses of IGBT 1 for normal D-PWM

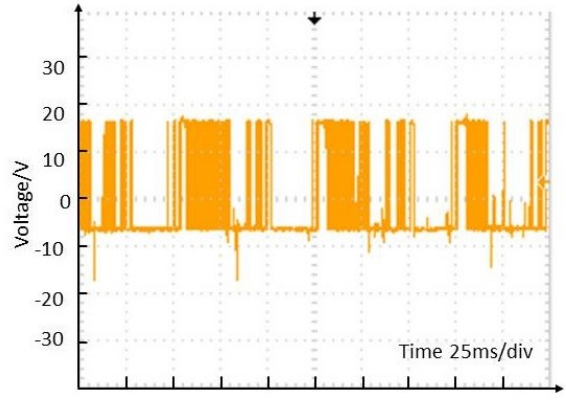

Figure 10. Firing pulses of IGBT 1 for operational map of type A

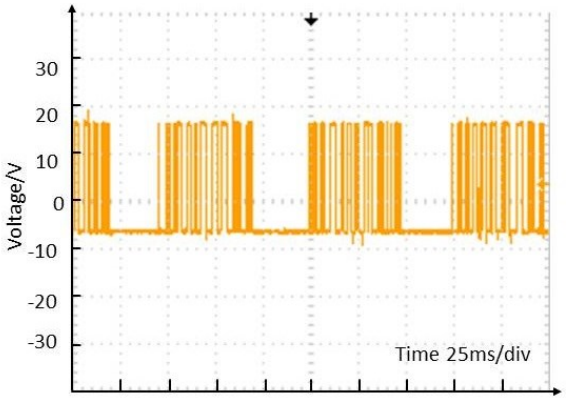

Figure 11. Firing pulses of IGBT 1 for operational map of type B

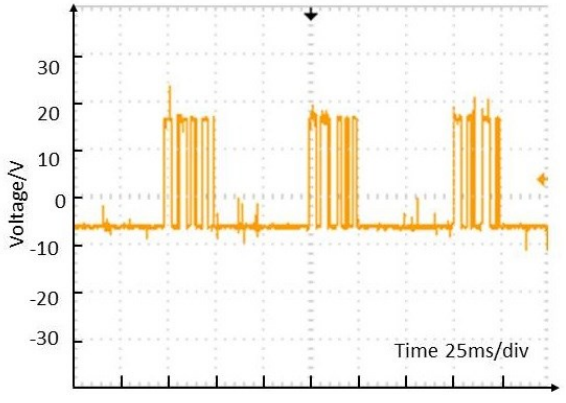

Figure 12. Firing pulses of IGBT 1 for operational map of type C

Fig. 9 to Fig. 12 show the firing pulses of the outer IGBT of the upper leg of phase U. As it can be seen, the pulse patterns are different in each of the operation modes. Therefore, it is expected that the losses of upper leg of phase U vary significantly depending on the operational map.

2) Neutral point performance

The neutral point voltage U_{np} is defined as:

$$U_{np} = U_{c1} - U_{c2}\ , \qquad (2)$$

the U_{c1} and U_{c2} refer to voltages of the upper and lower capacitors of the DC link as shown in Fig. 1.

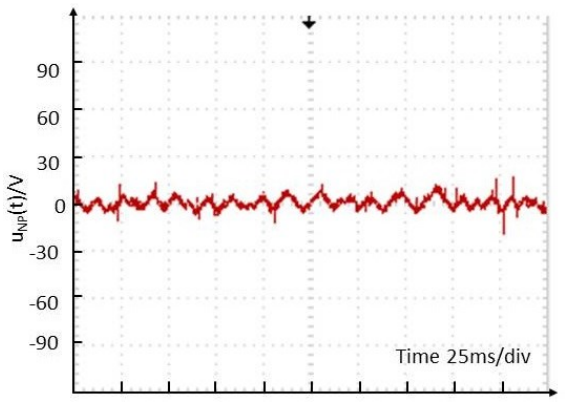

Figure 13. The neutral point voltage for normal D-PWM

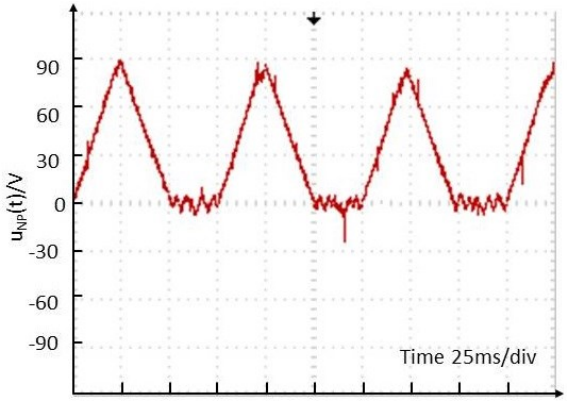

Figure 14. The neutral point voltage for operational map type A

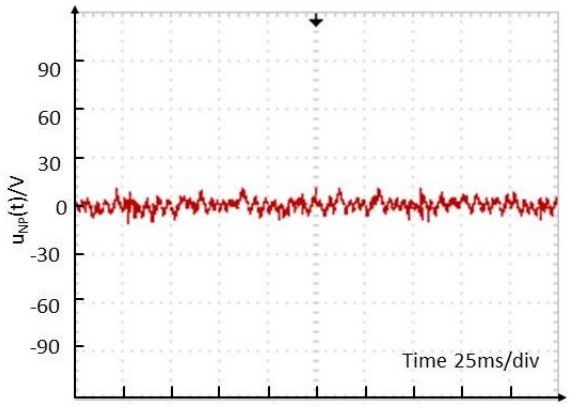

Figure 15. The neutral point voltage for operational map type B

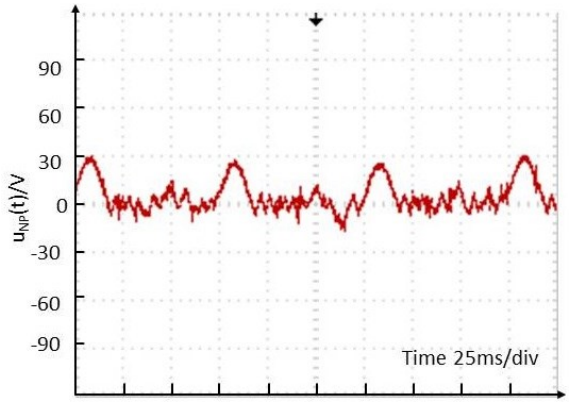

Figure 16. The neutral point voltage for operational map type C

As explained above, the performance of the control of the voltage of the neutral point of the dc-link has to be examined as well. Fig. 13 shows the voltage of the neutral point for the case of D-PWM and is quite low (2% of the dc-link voltage).

Conversely, in the case that the operational map of type A is applied, in which three switching vectors are excluded, the neutral point has the highest ripples (25% of the dc-link voltage) as it is shown in Fig. 14.

Fig. 15 depicts the performance of the neutral point, when the operational map of type B is applied, its performance becomes better and the ripple voltage is lower than in the previous case (3% of the dc-link voltage), because only one switching vector is excluded of the modulation. Thus, the effect of ALE on the control of the voltage of the neutral point of the inverter is minimized.

If the operational map of type B is changed to type C, where one or two switching vectors are removed from the calculation, the ripple of the neutral becomes larger as compared the B operation as it is shown in Fig. 16. Nevertheless the magnitude of the ripple of neutral point voltage is still acceptable (9% of the dc-link voltage).

3) Impact of ALE on the currents of the inverter

The modification of the PWM during the ALE operation of the inverter leads to asymmetries in the voltage of the inverter and in the currents of the machine. Therefore, the examination of the impact of ALE on the currents is essential for the overall assessment of the proposed modulation.

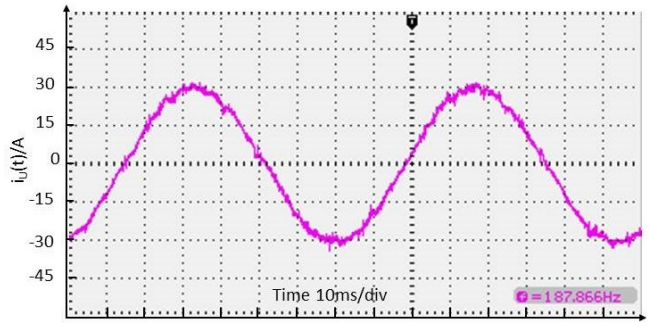

Figure 17. Stator current $i_u(t)$ for normal D-PWM

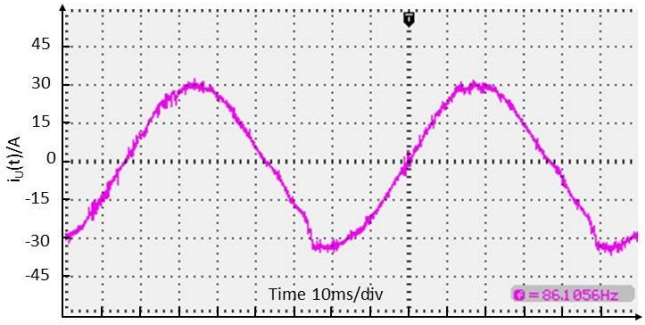

Figure 18. Stator current $i_u(t)$ for operational map type A

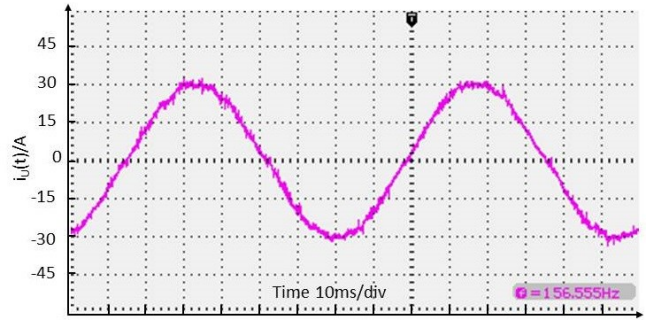

Figure 19. Stator current $i_u(t)$ for operational map type B

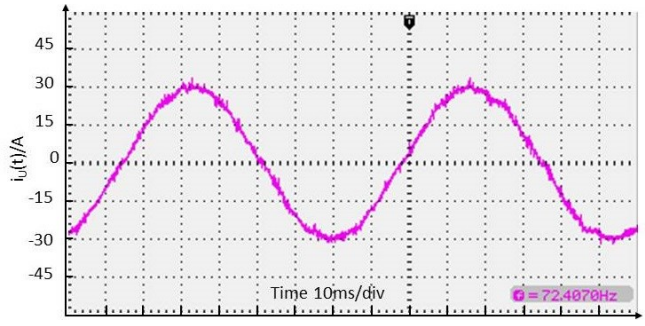

Figure 20. Stator current $i_u(t)$ for operational map type C

Fig. 17 shows the waveform of the stator current in normal operation with D-PWM and has a total harmonics distortion (THD) of 3.4%.

The waveforms of the stator current if applying the operational map of type B and of type C are shown in Fig. 19 and Fig. 20 respectively. Compared with the operation without ALE there is only a very small increase of the THD. The THD of the stator current is 3.4% with type B and 3.6% in case of operational map of type C. As shown above amplitude of the ripple on the voltage of the neutral point is kept in an acceptable range.

In contrast, as it is shown in Fig. 18, the waveform of the stator current for an operation with a map of type A is strongly distorted. The THD of the current is increased significantly to 7.3%. The ripple of on the voltage of the neutral point of the dc-link and the distortion of the currents are not acceptable and for these reasons, this kind of operation can be discarded.

4) The distribution of losses

In steady state, the over-temperatures of the heatsinks are directly proportional to total losses of each semiconductor device [8], hence the losses of semiconductors can be easily estimated by measuring the temperature of each heat sink. The temperature measurement with Pt1000 (Resistance Temperature Detectors) was preferred because it is reported that it is accurate, linear and stable over time and temperature and therefore better than thermistors, thermocouples or diodes [11].

Fig. 21 through Fig. 23 show the losses of each semiconductor device that were calculated based on the temperature measurement. The columns in blue represent the losses for discontinuous modulation (D-PWM), columns in red were measured in ALE operation.

Differently than expected the distribution of temperature respectively of the losses is not symmetrical in the three legs of the inverter. Although the setup has to be modified in order to get the same thermal conditions in all legs, the comparative results can be used for the evaluation of the performance of the proposal.

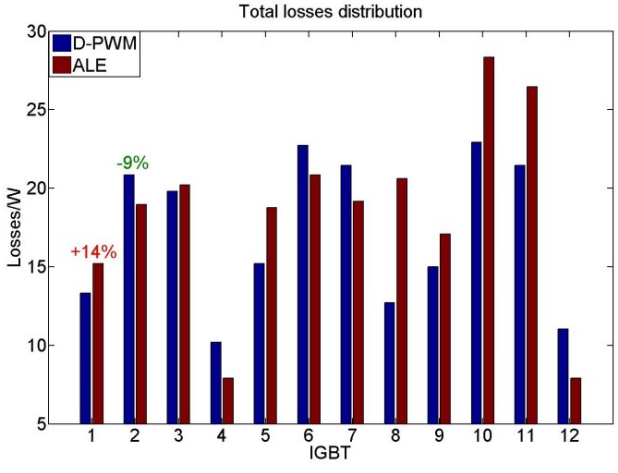

Figure 21. Operational map type A

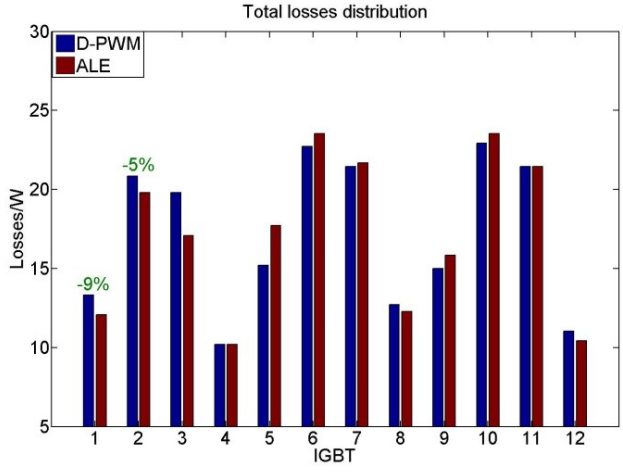

Figure 22. Operational map type B

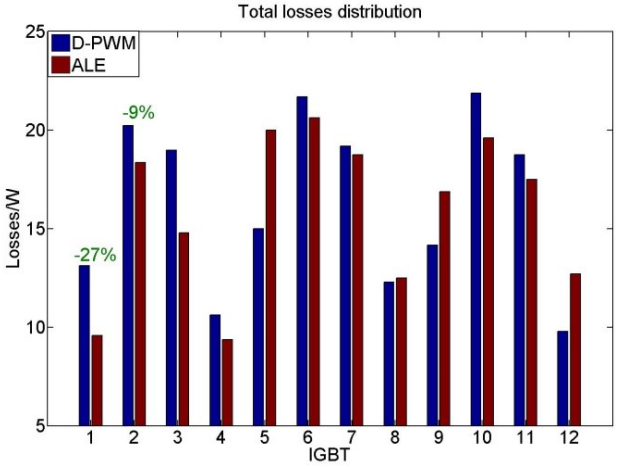

Figure 23. Operational map type C

Fig. 21 shows the loss distribution among the IGBTs under the following operation conditions: D-PWM (columns in blue) and ALE with operational map of type A (columns in red). As it can be seen in this result, the IGBT 2 benefits from the ALE strategy as losses of the semiconductor decreases for 9%. Conversely, the IGBT 1 suffers of higher losses that increase up to 14% if compared with the normal operation. These measurements illustrate that, the choice of the operational map is crucial for the effectiveness of the ALE in the range of low modulation index. An unsuitable selection of the operational map leads to lower thermal stress of the stressed device with the negative effect that other semiconductors are even exposed to higher thermal stress and the ripple of the neutral point will excessively increase. The overall performance of the system deteriorates significantly.

The loss distribution profile shown in Fig. 22 is very different, when the operational map type B is applied. Both IGBT 1 and IGBT 2 of the upper of phase U have fewer losses as compared with the normal operation. The performance of the neutral point voltage shown in Fig. 15 is also very good. It can be concluded that this mode of operation can be applied for long time to extend the lifetime of a semiconductor device exposed to an excessive heating and it features a minimum impact on the system performance.

If the operational map type B is still not sufficient to keep the upper leg of phase U under the thermal limit, the operational map type C can be used for the further reduction of the losses. It yields up to 27% fewer losses for IGBT 1 and 9% fewer losses for IGBT 2 as shown in Fig. 23. Nevertheless, this improvement is achieved at the cost of a higher ripple in the voltage of the neutral point than in case of operational map of type B.

IV. CONCLUSION

This paper continues the analysis and the experimental validation which begun in a previous work, in which a new concept for the redistribution of the power losses in a multilevel inverter is proposed for the case of a malfunction of control or of the cooling the inverter and consequently a local overheat-

ing of one of the semiconductor devices. Thus, the devised method aims at the active thermal protection and therefore the active lifetime extension of the particular stressed semiconductor switches. The performance of the proposed modulation scheme has now been examined and verified by experiments in a laboratory setup for the range of low modulation index. Thus the fault tolerant modulation can be applied in the complete voltage and current range of operation of the inverter. The impact of the proposed strategy on the neutral point potential balancing and on the quality of the phase currents was also investigated and shows a satisfactory operation when properly applied with three different operational maps. This concept is general and can be applied for any kind of multilevel inverter topology without the need of any additional hardware.

The ongoing work is dedicated to the enhancement of the modulation method by defining operational maps that are not necessary spaced in triangles of π /3 and by combining the modified modulation with a temperature control. The benefit of the methods in terms of life extension of the semiconductors will be also quantified.

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