PWM for Active Thermal Protection in Three Level Neutral Point Clamped Inverters

The-minh Phan[1], Gernot Riedel[2], Nikolaos Oikonomou[2], Mario Pacas[1]

theminh.phan@uni-siegen.de, gernot.riedel@ch.abb.com, nikolaos.oikonomou@ch.abb.com, pacas@uni-siegen.de

[1] Professorship for Power Electronics and Electrical Drives, Universität Siegen, Germany.

[2] ABB Corporate Research, Baden-Dättwil, Switzerland.

***Abstract*— In high power applications, in which the discrete power switches are mounted on separate heatsinks, an overload of a semiconductor device leads to a local excessive thermal stress and eventually to a failure of the system. Despite of a control strategy that ensures the even distribution of losses in the normal operation, a local thermal overload can arise due to failures in the electronics, in the cooling system, due to an inappropriate positioning of the semiconductor device, etc. In this paper, a new fault tolerant control approach is introduced to deal with this matter. When detecting increased thermal stress of one IGBT module, the switching strategy is altered in order to reduce the load of that particular IGBT module and to redistribute the losses and consequently the heat from the affected group or valve to the other switches. Hence, the temperature of the stressed switch is kept under the critical limit and the thermal overload is reduced. In such way the reliability and the lifetime of the converter is maximized even in case of thermal failure. In the proposed novel modulation concept, the balancing of the neutral point potential of the 3L-NPC Inverter is also ensured without any additional hardware.**

Keywords—Neutral point balancing, discontinuous PWM, space vector PWM, active lifetime extension, fault tolerant control

I. INTRODUCTION

There are many approaches to improve the distribution of losses among the semiconductors of 3L-NPC inverter. The most notable one is to add IGBTs antiparallel to the neutral point clamped diodes, this topology is known as 3L-ANPC (Active Neutral Point Clamped) inverter. The significant improvements in the thermal performance of the 3L-ANPC inverter have been proven by various researchers [2]-[7][11]. Yet the adaptation of existing 3L-NPC inverters into 3L-ANPC is not always feasible due to higher cost that results from additional hardware. Hence numerous 3L-NPC inverters in operation in the field do not have any benefit from this approach and are still vulnerable to the local thermal overload.

The redundant voltage space phasors that are available in the 3L-NPC inverter can be used to balance the neutral point or for the reduction of the common mode voltage. Their utilization for the management of the losses in the semiconductor devices was first mentioned in [1]. The approach presented there takes advantage of the redundant space phasors to actively redistribute losses from a thermally overloaded semiconductor to the others; hence the active thermal protection is directly achieved. Moreover, as a long term effect, the expected lifetime of the especially stressed components is extended significantly. Therefore this strategy was named ALE (active lifetime extension). As the neutral point must be also controlled by using the same redundant space phasors, a trade-off between the loss redistribution concept and the neutral point control mechanism is needed in order to ensure the proper function of the system. Obviously, this approach yields no additional expenses or changes in the hardware and therefore it can be applied directly to any 3L-NPC inverter in operation. This present work is an extension of the concept described in [1] for the high modulation range, in which the number of the redundant states of inverter for a given voltage space phasor decreases. Therefore the ALE strategy presented there has been modified and enhanced as described in the following.

II. PWM STRATEGY FOR REDISTRIBUTION OF LOSSES

For a basic analysis, it is sufficient to consider the upper leg of phase *U* of the inverter, which is depicted with red color in Fig. 1 as the hotspot i.e. the group of overheated devices, in which the thermal load has to be reduced. The modulation index m ($0 \le m \le 1$), which is considered in the following is defined as:

$$m = \frac{U_{phase}}{U_d/\sqrt{3}}, \tag{1}$$

where U_{phase} is the amplitude of phase voltage and U_d is the DC–link voltage of the 3L-NPC inverter. For the subsequent analysis, only the operation of the inverter in the higher modulation range $0.5 < m \le 1$, is examined. The modulation range $0 < m \le 0.5$, described in [1], is solely relevant in starting-up phase of the simulations carried out for the present work and it is not investigated further.

The output potential of each phase can acquire three discrete levels, $+u_d/2$, 0, or $-u_d/2$, depending on the control of the four power switches in the respective phase arm. Three different states are therefore identified for each phase; they are explained with reference to phase *U*:

- Positive output potential: If switches S1 and S2 are turned on, the phase *U* potential $u_U = +u_d/2$.

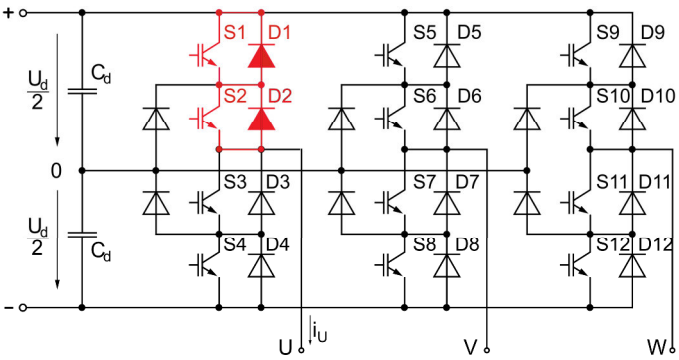

Fig. 1. Neutral Point Clamped Inverter

- Zero output potential: If switches S_2 and S_3 are turned on, then $u_U = 0$.
- Negative output potential: If switches S_3 and S_4 are turned on, then $u_U = -u_d/2$.

A total of 27 different arrangements of the switches are therefore possible. They are selected by the firing signals at the gates of the power semiconductors.

Each arrangement stands for a respective voltage space phasor or a switching state vector. The voltage space phasors of the three-level inverter are shown in Fig. 3. The notation, e.g. (+,0,–), indicates that phase U is connected to the positive DC rail, phase V is connected to the neutral point 0, and phase W is linked to the negative dc rail. Each phasor is characterized by its intensity and orientation in the complex plane.

The voltage space phasors, Fig. 3, can be listed in four categories: (i) "small" phasors, such as $u_1^+(+,0,0) \parallel u_1^-(0,-,-)$, which exhibit single redundancy; the two redundant forms contribute to the same terminal voltage at the inverter terminals, (ii) "medium" phasors, such as (+,0, –) that connect only one output terminal to the neutral point of the inverter, (iii) "large" phasors , which exhibit no redundancy, connect each output terminal either to the positive or to the negative dc rail, and (iv) the zero phasor that exhibits double redundancy.

A. Reduction of losses by using redundant states

The thermal losses of a semiconductor device consist of switching- and conduction losses. In the following the effect of using the redundant voltage space phasors on each of these types of losses will be considered.

As stated above in the present work an overload of the upper leg of phase U in the modulation range $0.5 < m \leq 1$ is examined. Therefore it is only necessary to consider the voltage phase phasors that are located in the blue area of Fig. 3, as only in this region the losses of the upper leg of phase U can be influenced by choosing the appropriate redundant state. So in the strategy proposed in the following the pulse width modulation for voltage space phasors located in the white areas of Fig. 3 is not modified.

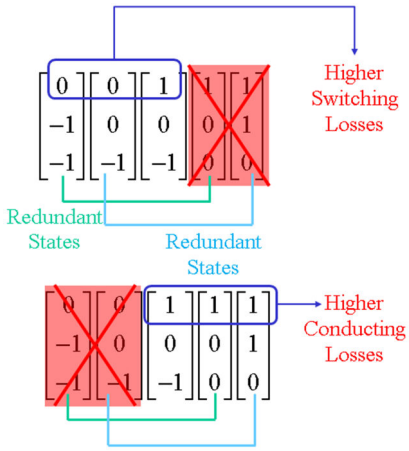

Fig. 2: Redundant states and their impact on the losses

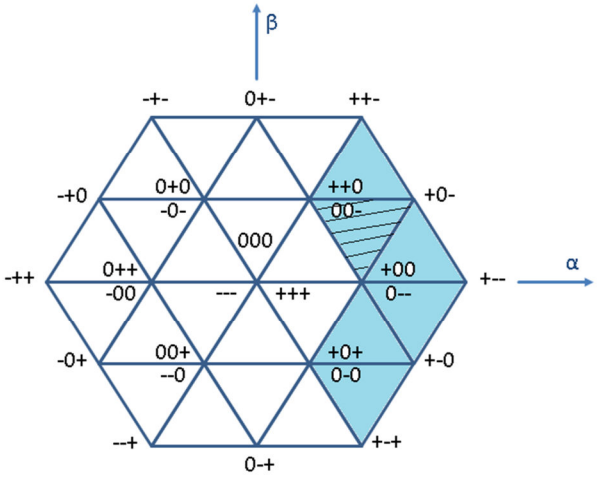

Fig. 3. Operation map

1) Reduction of conduction losses

The upper part of Fig. 2 shows, as an example, the switching states that correspond to the voltage space phasors located in the corners of the shaded triangle in Fig. 3. When discontinuous PWM [9] is employed, all three of them are used to synthesize an output space phasor located within this triangle and to build the respective switching pattern. To reduce the conduction losses of the upper leg of phase U, it is necessary to avoid using the states depicted in red, in which phase U is clamped to the positive DC bus. Of course, the reduction of losses depends on the modulation index and on the conduction times associated with the pulse pattern. Unfortunately a reduction of conduction losses in this way implies an increase of the switching losses in the same semiconductor.

2) Reduction of switching losses

The lower part of Fig. 2 shows the complementary case, in which the switching losses can be reduced by utilizing switching sequences, in which phase U is kept connected to the positive DC bus and by avoiding the states marked in red. By favoring these sequences, it is obvious that the conduction losses increase due to longer on-time of the corresponding semiconductor.

3) Reduction of overall losses in the high modulation range

As explained above a strategy of reduction of losses exhibits competing goals and leads therefore to a dilemma as the reduction of the conduction losses leads to higher switching losses and vice versa. Thus, a simple approach is not possible and the consideration of other aspects is mandatory. The operation of the inverter at higher output voltages yields sequences of switching states, in which the on-time of the redundant space phasors decreases with increasing modulation index. The potential for the reduction of conduction losses by exploiting the corresponding sequences is therefore quite limited. In contrast to this, the reduction of the switching losses is independent of the on-times of the redundant states in the corresponding sequences. Furthermore the switching losses in power semiconductor devices for medium voltage applications are particularly high. Hence, the reduction of switching losses is preferred in this region of operation regardless of the higher conduction losses. As it will be shown in the following, the reduction of the overall losses is still achieved with this strategy.

B. *Trade-off between neutral point balancing and loss distribution by using redundant states*

The neutral point balancing and the loss distribution issues are concurrent optimization targets both demanding the utilization of redundant states of the inverter. The situation is worsened particularly in the higher modulation range, in which the availability of redundant states declines. Therefore, this paper proposes a solution for the arbitration of this conflict. Fig. 3 shows the blue area where the ALE strategy for the loss redistribution is applied to the upper leg of phase *U*. As long as the reference voltage phasor is located in this area and a thermal overload in the upper leg of phase *U* occurs, ALE has priority and the control of the neutral point voltage is deactivated. Yet the neutral point is continuously monitored and in case that its potential crosses a predefined threshold, the priority of ALE is lost and the neutral point control is reactivated. As explained at the beginning of this section in the inner hexagon of the white colored region ALE is not active because $0 < m \leq 0.5$, which is not taken into account in this paper. In the other white areas the losses of U are not affected by the modulation and ALE does not apply. In both cases the redundant states can be used for the balancing of the neutral point of the inverter.

The Fig. 4 shows the scheme for the realization of the ALE strategy to control the 3L-NPC inverter. The reference voltages for all three phases are obtained from the current controllers, they are converted to two phases (α,β-coordinates) and are fed to the space vector PWM algorithm described in [14] to calculate all the switching states with their corresponding on-times. These are formed to a switching matrix, as shown in Fig. 2. The switching states are arranged so, that they require *only one* switching action for the transition between two adjacent switching states, thus the optimum space phasor sequences [16] are achieved.

In the normal operation mode, the procedure continues directly after calculation of the switching matrix with the neutral point balancing algorithm [15] to choose an optimum set of switching states to control the neutral point potential. This optimum set consists of three as well as four switching states for discontinuous PWM or for continuous PWM [9].

If a thermal overload is detected, the ALE operation is initiated and the proposed procedure optimizes the switching patterns by removing all the *harmful* switching states that cause thermal stress. A switching strategy decides which switching states are *harmful* depending on the losses that they produce. If the conduction losses have to be reduced the switching states yielding higher conduction losses are eliminated from the switching matrix. Conversely, if the reduction of switching losses has the priority the corresponding states are forbidden. As the upper part of Fig. 2 shows the case in which the states $[1\ 0\ 0]^T$ and $[1\ 1\ 0]^T$ are eliminated of the switching matrix in order to reduce the conduction losses on the upper leg of phase *U*. The remaining states have lower conduction losses at the expense of higher switching losses. The lower part of Fig. 2 illustrates the case in which the states $[0\ -1\ -1]^T$ and $[0\ 0\ -1]^T$ are forbidden so that the switching losses *on the upper leg of phase U* decrease and the conduction losses increase.

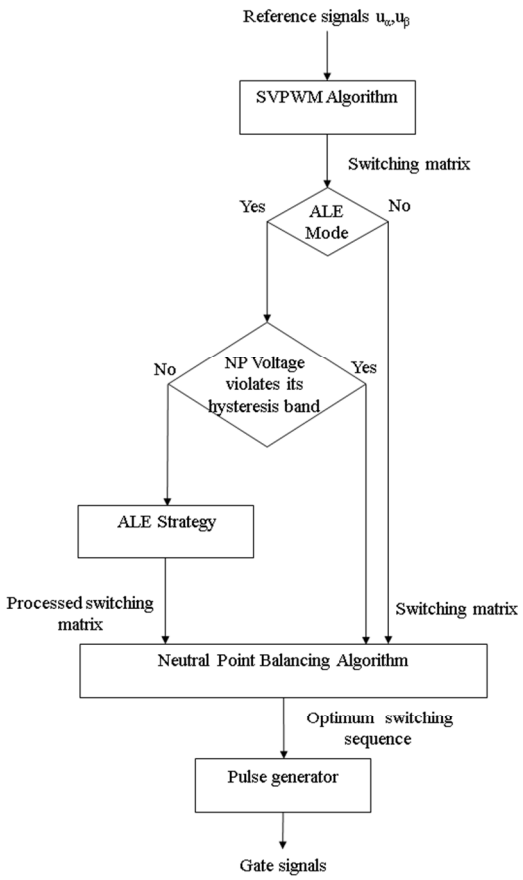

Fig. 4. ALE control scheme

If the desired voltage space vector is located in the white areas depicted in Fig.3, the switching matrix is taken as computed, the ALE procedure is ignored and the PWM proceeds without any change with the algorithm for the balancing of the neutral point.

In the modulation range $0 < m \leq 0.5$, not considered in the present work, both the control of the neutral point voltage and the ALE strategy can be applied simultaneously as enough switching states are available. Yet in the operation range of $0.5 < m \leq 1$ the ALE procedure forbids some of the redundant switching states, so only three switching states remain that are not sufficient for the control of the neutral point voltage, thus this step in the flow diagram in Fig. 4 is bypassed and the algorithm goes directly to the pulse generator.

III. Loss Calculation

For a first theoretical validation of the proposed enhanced switching strategy a calculation of the losses is used. The method for modeling of the losses of the semiconductor devices described in [8] provides good accuracy with moderate calculation efforts. The conduction losses of IGBTs are calculated as:

$$P_{conduct} = U_{CE}.I_C = \left(U_{CE,0} + I_C \cdot r_{CE}\right) \cdot I_C, \quad (2)$$

I_C denotes the instant collector current through the IGBT. The Collector-Emitter voltage $U_{CE,o}$ and the differential resistance r_{CE} are extracted directly from the on-state characteristics curve. The calculation of the switching loss energy in IGBTs is formulated as:

$$E_{switch} = E_{switch,0} \cdot \frac{U_{dc}/2}{U_{base}} \cdot \frac{I_C}{I_{C,base}}, \quad (3)$$

the base switching loss $E_{switch,0}$ is obtained from data sheet for a given condition with the base commutation voltage of U_{base} and with base collector current of $I_{C,base}$. Obviously, every IGBT of the 3L-NPC inverter must withstand the maximum commutation voltage of $U_{dc}/2$. The E_{switch} stands for either turn-on or turn-off loss energy. The average switching loss power is derived subsequently as (4), if switching frequency of inverter is known.

$$P_{switch} = f_{switch} \cdot E_{switch,} \quad (4)$$

finally the overall losses is computed as the sum of all losses:

$$P = P_{conduct} + P_{switch,on} + P_{switch,off}. \quad (5)$$

In a similar manner, the conduction losses and recovery losses of Diode are easily calculated with (2-5).

IV. Results

To verify the proposed modulation scheme, a medium voltage induction machine (U_n = 3000V, P_n = 560kW) fed by a 3L-NPC inverter (U_{dc} = 4670V, C_{dc} = 3.8mF, switching frequency = 1000Hz) is first investigated by means of simulation for rated operation with m = 0.97 and $cos\varphi$ = 0.84. The numbering rule for the semiconductors devices is shown in Fig. 1. The calculations were carried out by assuming IGBTs with data according to [12].

Fig. 5 depicts the conduction losses of all IGBT switches (numbering as in Fig. 1) for three different cases: for normal operation with continuous PWM (C-PWM) as blue columns, for normal operation with discontinuous PWM (D-PWM) as green columns and for ALE operation with discontinuous PWM in red [9]. The grey columns show the corresponding switching losses in each particular operation mode. It can be seen that the overall losses in switch 1 in ALE operation has been reduced to approximately 50 % of the losses in normal operation.

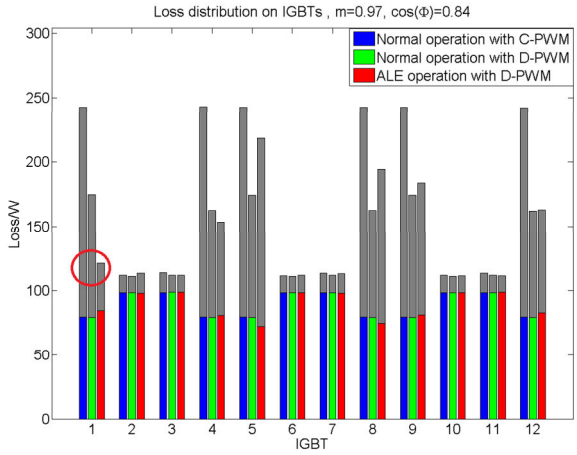

Fig. 5. Loss redistribution performance on IGBTs. RGB columns: conduction losses; Grey columns: switching losses.

Despite of the reduced availability of redundant states at high modulation index m = 0.97, the ALE strategy is successfully applied by transferring the losses to other switches i.e. 5 and 8 with their consequent increase of temperature that has to be considered in the whole thermal household of the inverter. Thanks to the significant loss reduction the ALE strategy can extend considerably the expected lifetime of a particularly stressed switch and the probability of system survival can be greatly improved. A quantification of the reliability improvement of the inverter as described in section II.D of [1] belongs to the works under examination.

Fig. 6 shows no considerable increase of the losses among the antiparallel Diodes of the corresponding IGBTs. In the inverter operation, the main part of losses is caused by the IGBTs and not by the freewheeling diodes, therefore the reduction of the losses in the IGBTs results in a reduction of the thermal stress of the freewheeling diodes as an additional benefit of ALE.

In order to verify that the strategy of the reduction of switching losses is the proper one an inverter equipped with IGBTs with data as in [12] was simulated in a further step for

a variable speed operation and a mechanical load according to the characteristic $M_{load} = M_{rated} \cdot (n / n_{rated})^2$.

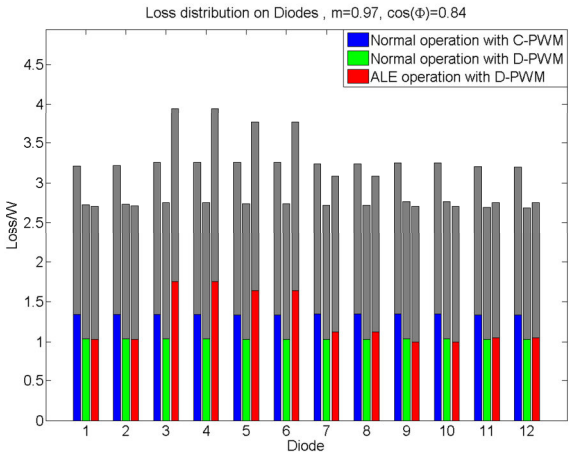

Fig. 6. Loss redistribution performance on Diodes. RGB columns: conduction losses; Grey columns: switching losses.

For this operation the overall losses on the upper leg of phase *U* is plotted in Fig. 7 for both a switching strategy with reduction of switching losses in blue and one yielding the reduction of conduction losses in red. It can be seen that the strategy with reduction of switching losses, as proposed above, leads to a reduction of the overall losses over a wide speed range.

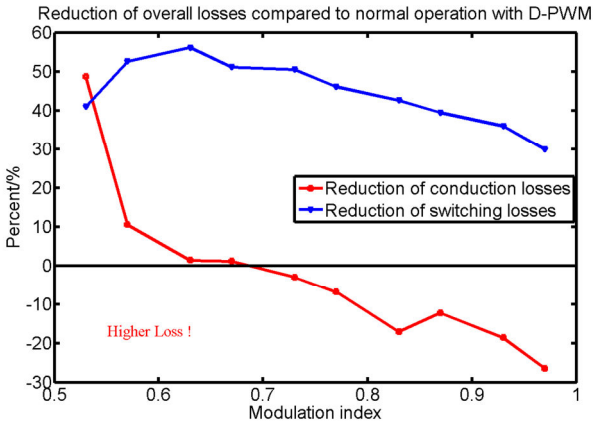

Fig. 7. The advantage of reduction of switching losses strategy

In order to ensure the effectiveness of the proposed strategy in the case of IGBTs with different characteristics the case examined above was considered again at the same test conditions yet with a different type of IGBT [13], which has lower switching losses in cost of higher conduction losses compared to the counterpart [12]. The results are plotted in Fig. 8. Obviously, the capability of the switching losses reduction is lower as the one depicted in Fig. 7 but its superiority over the strategy with reduction of conduction losses is still preserved in the modulation index range above m = 0.52.

Fig. 8. The performance of ALE strategy

The performance of the neutral point in ALE operation is depicted in the lower trace of Fig. 9. By analyzing the spectrum of the neutral point, besides the 3rd harmonic component that is dominant in the spectrum of the neutral point potential, also additional harmonics (1st, 2nd, 4th, 5th, 7th) and even a DC offset voltage appear in the neutral point potential.

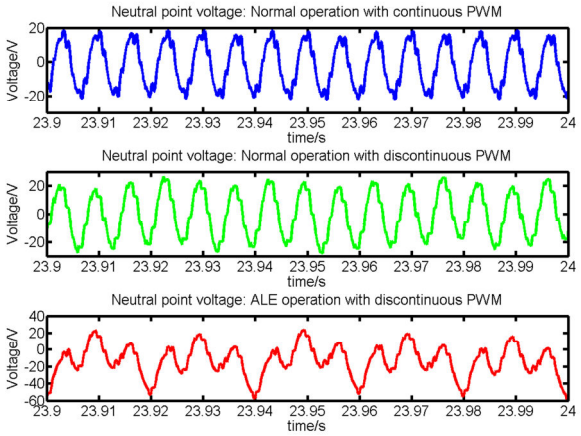

Fig. 9. Neutral point performance, m=0.97, cosφ=0.84

The appearance of the odd harmonics 1st, 5th, 7th and of the DC offset is as a consequence of the ALE strategy that causes irregular interruptions of the control of the neutral point voltage. The even harmonics, i.e. the 2nd and the 4th, are a result of the DC offset voltage due to the self-balancing effect [10] of 3L-NPC. Nevertheless the neutral point voltage is kept stable yet with a higher ripple.

Fig. 10 shows the impact of ALE on the balancing of the neutral point for different operating conditions. Hereby a quadratic load $M_{load} = M_{rated} \cdot (n / n_{rated})^2$ is assumed. It can be seen that the ripple of the neutral point voltage with ALE (red curve) is larger compared to normal operation. The higher amount of harmonics in the neutral point increases also the total harmonics distortion, this effect is being under

investigation. Despite of these the loss reduction in the IGBTs is significant.

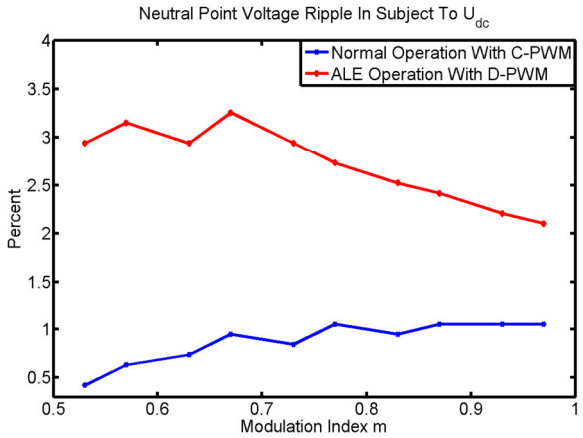

Fig. 10. Performance by various operation points

The simulation results verify the satisfactory operation of the ALE based control in a wide speed range. After the successful conclusion of the preliminary study a laboratory set-up is now being built in order to get the experimental confirmation of the effectiveness of the proposed strategy.

V. CONCLUSIONS

In this paper, a new modulation strategy is presented aiming a fault tolerant control of the 3L-NPC inverter in case of a local thermal overload (hotspot) due to a failure. The modulation actively protects switches that are suffering overload and reduces their respective losses. Its performance for the whole operation range has been investigated by means of calculations and simulations. This study confirms the possibility of significant loss redistribution on the selected semiconductor device for a wide modulation range by using the redundant states of the inverter. The impact of this concept on the neutral point balancing was also investigated and shows a satisfactory operation if properly applied. The ongoing work is dedicated to the experimental verification of the proposed strategy as well as for the quantification of the improvement in the reliability of the inverter. The presented concept is a novel generic approach, which is applicable to any multilevel topology.

REFERENCES

[1] G. Riedel, N. Oikonomou, R. Schmidt und D. Cottet, “Active lifetime extension — Demonstrated for voltage source converters“, Electrical and Electronics Engineers in Israel (IEEEI), 2010 IEEE 26th Convention of , vol., no., pp.000530-000534, 17-20 Nov. 2010.

[2] T. Bruckner, S. Bernet and H. Guldner, “The active NPC converter and its loss-balancing control“.Industrial Electronics, IEEE Transactions on, vol.52, no.3, pp. 855-868, June 2005.

[3] Bruckner, T.; Bernet, S.; Steimer, P.K., "Feedforward Loss Control of Three-Level Active NPC Converters," Industry Applications, IEEE Transactions on , vol.43, no.6, pp.1588,1596, Nov.-dec. 2007 doi: 10.1109/TIA.2007.908164

[4] D. Andler, J. Weber, S. Bernet and J. Rodríguez, "Improved model predictive control with loss energy awareness of a 3L-ANPC voltage source converter".Applied Electronics (AE), 2010 International Conference on , vol., no., pp.1-6, 8-9 Sept. 2010.

[5] ANDLER, D.; Hauk, E.; Alvarez, R.; Weber, J.; Bernet, S.; Rodriguez, J., "New junction temperature balancing method for a three level active NPC converter," *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on* , vol., no., pp.1,9, Aug. 30 2011-Sept. 1 2011

[6] D. Floricau, E. Floricau and G. Gateau, “Three-level active NPC converter: PWM strategies and loss distribution“. Industrial Electronics, 2008. IECON 2008. 34th Annual Conference of IEEE, vol., no., pp.3333-3338, 10-13 Nov. 2008.

[7] Floricau, D.; Floricau, E.; Parvulescu, L.; Gateau, G., "Loss balancing for Active-NPC and Active-Stacked-NPC multilevel converters," *Optimization of Electrical and Electronic Equipment (OPTIM), 2010 12th International Conference on* , vol., no., pp.625,630, 20-22 May 2010

[8] M. Bierhoff and F. Fuchs, “Semiconductor losses in voltage source and current source IGBT converters based on analytical derivation“.Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual, vol.4, no., pp. 2836- 2842 Vol.4, 2004.

[9] T. Bruckner and D. Holmes, “Optimal pulse-width modulation for three-level inverters,“.Power Electronics, IEEE Transactions on , vol.20, no.1, pp. 82- 89, Jan. 2005.

[10] J. Shen, S. Schröder, R. Rösner and S. El-Barbari, “A Comprehensive Study of Neutral-Point Self-Balancing Effect in Neutral-Point-Clamped Three-Level Inverters“.Power Electronics, IEEE Transactions on , vol.26, no.11, pp.3084-3095, Nov. 2011.

[11] Rodriguez, J.; Bernet, S.; Steimer, P.K.; Lizama, I.E.;, "A Survey on Neutral-Point-Clamped Inverters," Industrial Electronics, IEEE Transactions on , vol.57, no.7, pp.2219-2230, July 2010.

[12] HiPak IGBT Module 5SNG 0250P330305, datasheet information.

[13] Eupec IGBT Module FF200R33KF2C, datasheet information.

[14] Celanovic, N.; Boroyevich, D.; “A fast space-vector modulation algorithm for multilevel three-phase converters”, Industry Applications, IEEE Transactions on , vol.37, no.2, pp.637-641, Mar/Apr 2001.

[15] Holtz, J.; Oikonomou, N.; “Neutral Point Potential Balancing Algorithm at Low Modulation Index for Three-Level Inverter Medium-Voltage Drives”, Industry Applications, IEEE Transactions on , vol.43, no.3, pp.761-768, May-june 2007.

[16] McGrath, B.P.; Holmes, D.G.; Lipo, T., "Optimized space vector switching sequences for multilevel inverters," *Power Electronics, IEEE Transactions on* , vol.18, no.6, pp.1293,1301, Nov. 2003.