Increasing the Efficiency of a Single Phase Z-Source Inverter by utilizing SiC – MOSFETS

Dipl.-Ing. Manuel Steinbring, Universität Siegen, Hölderlinstraße 3, 57068 Siegen, Germany
manuel.steinbring@uni-siegen.de

Univ.-Prof. Dr.-Ing. Mario Pacas, Universität Siegen, Hölderlinstraße 3, 57068 Siegen, Germany
pacas@uni-siegen.de

1. Abstract

Earlier implementations of a single phase Z-Source inverter which were examined in a laboratory set-up have shown a satisfactory behavior with good dynamic performance. However, the major disadvantage was the resulting low efficiency of the whole energy conversion system. In this paper it is shown that the efficiency of the ZSI can be enhanced by replacing the standard Si-IGBTs by new SiC (Silicon Carbide) MOSFETS. In this way the switching losses in the semiconductors can be significantly reduced. The total losses decrease up to 35 % achieving an efficiency improvement of up to 10 %.

2. Introduction

In comparison to standard inverter topologies, a Z-Source inverter (ZSI) is equipped with a modified DC-link. By adding two inductors to the DC-link the ZSI is capable of boosting the input voltage without the need of a second input boosting stage. The ZSI also features fault tolerance capability (e.g. in case of DC-link shoot trough) which makes it ideal for operation in harsh environments as they are found in very small hydro-generators located in outlying regions. In previous papers [1] [2] a single phase output ZSI has been proposed. The first developed prototype worked well and could cope with a widely varying input voltage. Unfortunately, its main drawback was the poor overall efficiency of the system. Even under good operating conditions, i.e high input voltage, it barely reaches 90% efficiency dropping down to 68 % in unfavorable conditions. Therefore, in a further step of development the standard SI – IGBT were replaced by SiC MOSFETs in order to improve the efficiency of the ZSI.
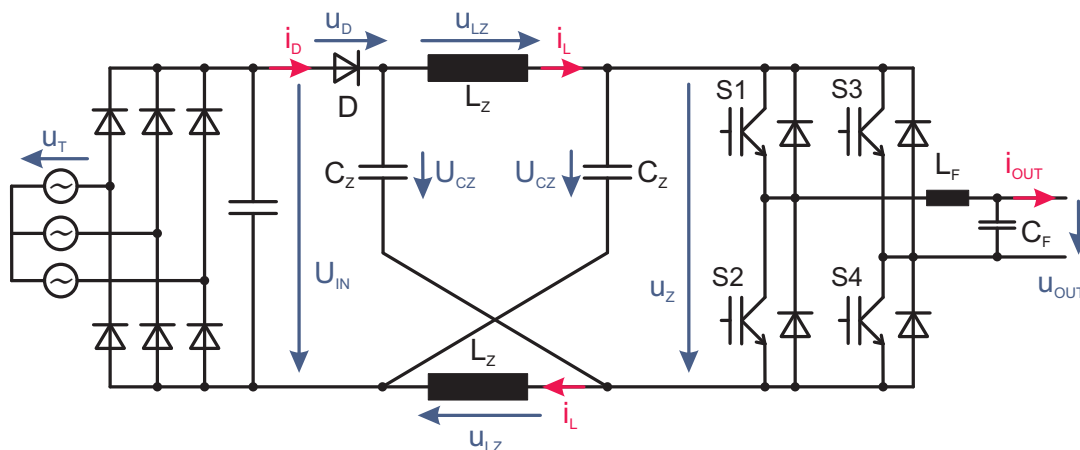

Figure 1: The complete circuit of the proposed ZSI

3. Circuit analysis and control structure of the Z-Source Inverter

The circuit of the utilized ZSI is depicted in Figure 1. A variable transformer connected to a rectifier was used to provide the input voltage. This allows a variable input voltage and the operation of the inverter in defined conditions.

As described in previous papers [1] - [4] for controlling the ZSI three switching states of the inverter are used. The most important state is a short circuit (shoot trough) at the output of the inverter. Due to the additional inductors in the DC-link this shoot through will not cause damage to the inverter. In this state the capacitors are parallel to the inductor which causes the current through the inductors to increase and transfer energy from the capacitors to the inductors. The longer the short circuit is the higher the boosting of the ZSI.

The remaining time within a switching period is available for an active state and for a freewheeling state in the inverter. In the active state two diagonal switches of the H-bridge are closed. Now the current flowing through the inductors drops which leads to a $\dfrac{di_L}{dt}$ that gives a voltage boost from the inductors. Together with U_{CZ} a higher voltage compared to U_{IN} is generated that can now be applied to the load.

The freewheeling state provides a path for both the load current and the inverter current by closing either the upper or the lower switches of each leg. This state is required to fill up the switching period in single phase ZSI as shooting and active time do not always add up to a 100 % duty cycle.

The output voltage of the ZSI depends on the shoot through time respectively on the relative shoot through time or duty cycle and the modulation index of the PWM. The overall boosting B_B of the ZSI and can be described by the well-known equation:

$$B_B = B \cdot M_{MAX} = \frac{1}{1 - 2D_S} \cdot (1 - D_S) \qquad (1.1)$$

Therein B_B is the maximum overall achievable voltage boost, B is the boosting correlated to the shoot through, M_{MAX} is the achievable maximum modulation index and D_S is the shoot through duty cycle. As the relative shoot through D_S is within the switching period of the Pulse Width Modulation (PWM), the maximum achievable modulation index is reduced accordingly. The effect which is produced by the boosting is greater than the reduction of the output voltage u_{OUT} caused by the reduced modulation index. By this an overall boosting can
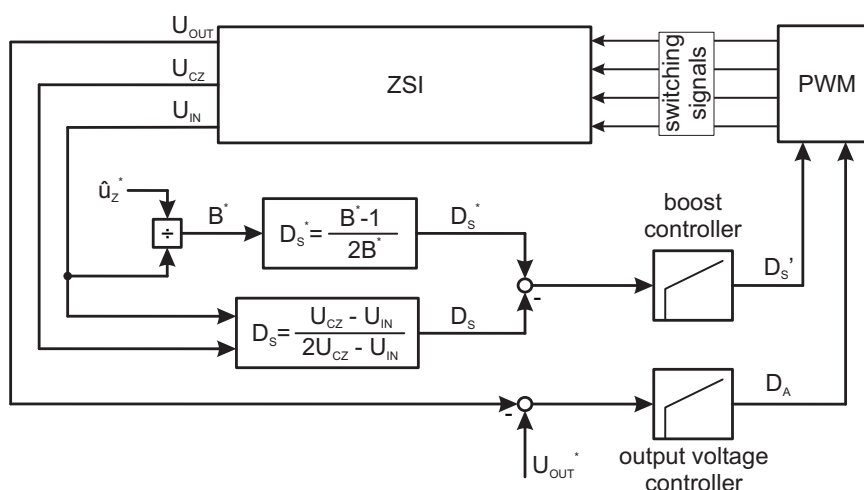

Figure 2: Proposed control structure for the ZSI with a dedicated controller for the boosting and for the output voltage.

707

still be achieved. This can be seen in the last part of the equation (1.1).

For the single phase ZSI a special control scheme is proposed which consists of two controllers as it is depicted in Figure 2 and in which the voltage control and the boosting are separated of each other. The first controller computes the boosting of the ZSI and according to (1.1) the shoot through duty cycle D_S. First the reference value for the boost (shoot through) duty cycle D_S^* is calculated by dividing the required output voltage u_Z by the input voltage U_{IN}. The input voltage U_{IN} and the voltage U_{CZ} on the capacitor are used for the calculation of the actual D_S which is compared with the set point value. The difference is fed into the PI-boost controller that corrects the shoot through duty cycle to the desired value. Thus the simple open-loop calculation is improved.

In certain conditions the ZSI inverter operates in discontinuous conduction mode, in which the current through the inductor L_Z is not changing so the $\frac{di_L}{dt}$ is zero and the voltage $û_Z$ is less than expected. In the first stage of the experimental work the control of the output voltage was without any feedback (open loop). Besides, the discontinuous mode was not detected; therefore the output voltage could not reach the set point value. Under unfavorable conditions, the voltage U_{OUT} dropped to 190 V RMS. For these reasons an output voltage controller was introduced for the control of the active state duty cycle D_A and in this way of the output voltage. By using this control strategy, the output voltage is kept constant at 230 V RMS regardless the conditions of the ZSI. The German grid requirements [6] can be fulfilled.

The outputs of the controllers deliver the values of D_S and D_A to the PWM that generates the switching signals. The calculated shooting time is applied as a negative dead time. By doing so, the shoot through can be easily included in the PWM-scheme and the number of switching transitions is not increased compared to standard voltage source inverter topologies.
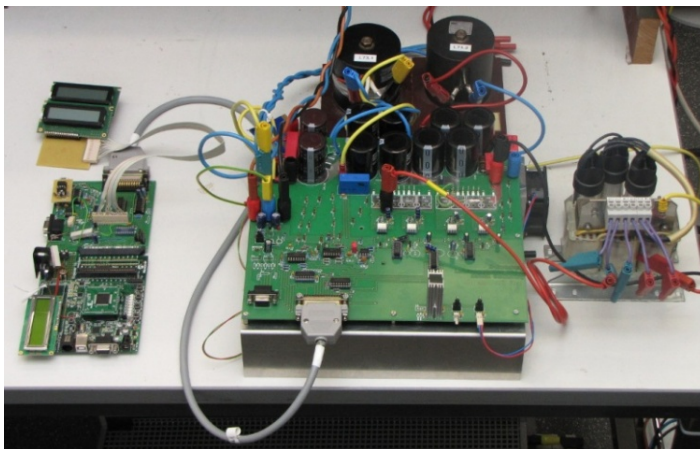

Figure 3: Laboratory setup of the ZSI

Rated output power	1.5 kW
Output voltage	230 V RMS, 50 Hz AC
Inductance L_Z	1 mH
Capacitance C_Z	470 µF

Table 1: Data of the laboratory setup

4.   The experimental setup

As stated in [1], the losses occurring in the semiconductors have the major influence on the losses of the ZSI. By replacing the standard semiconductor switches with SiC-transistors the losses can be reduced and the overall efficiency increased. The utilized setup is similar to the one proposed in [1]. It is a lab-design and consists of two boards. The main board contains the measurement- and gate driving circuit and the actual ZSI. This board is connected to a controller bard with a DSPic Microcontroller onboard to control the ZSI. For the new examined setup, only the semiconductor devices have been substituted. Two similar

setups were built up; one was equipped with IXYS IXA27IF1200HJ IGBT and the other one with Cree CMF20120D SiC – MOSFETS. The input diode was also replaced by a SiC type. A simple resistor was used as a load. Both the input and the output power were measured and the efficiency was calculated based on these data. A Norma D6100 wideband power analyzer was used to measure the input power. It has an accuracy of 0.1 % for power measurement. For determining the output power the voltage u_{OUT} and the current i_{OUT} where measured separately. As the load is only ohmic the simple multiplication of both values gives the power. The output voltage was measured with a high precision voltmeter and double checked with a transient recorder with a resolution of 12 bit. The current measurement was performed with a shunt and a multimeter. Again the value was double checked with an ampere meter which has an accuracy of 0.2 %. As a result the output power could be measured with an accuracy of at least 0.1 %. Figure 3 shows the laboratory setup and Table 1 lists up the most important data of the setup.
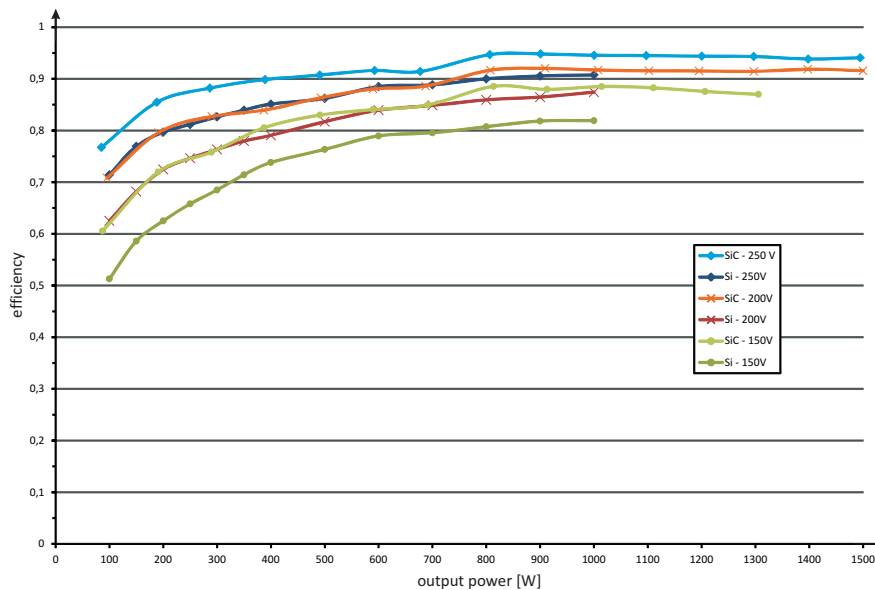

Figure 4: Comparison of the efficiency of the Si and SiC equipped ZSI

5. Experimental Results

To compare the performance of the semiconductors, the same measurements were performed with both setups. First the input voltage was held at a constant level and the power consumed in the load was increased in increments of 50 W respectively 100 W. This was done for different input voltages keeping the switching frequency for both setups at 9 kHz. Figure 4 shows that a simple change of the semiconductors has a significant effect on the efficiency. The increase in efficiency is 6 % when the ZSI is operated at an input voltage of U_{IN} = 150 V (green curves). This increase in efficiency can be achieved throughout the whole output power range. The maximum efficiency increase is 10 %. Speaking in terms of absolute losses they can be reduced by 15 to 30 %. If the input voltage is increased the benefit of the SiC semiconductors is reduced but still clearly noticeable. At U_{IN} = 200 V the increase in efficiency is at about 5 % (red and orange curves), for U_{IN} = 250 V the increase shrinks to 4 % (blue curves). Again the benefit appears throughout the whole power range. It is also noticeable that the maximum output power which can be delivered by the circuit is increased.

To analyze the influence of the switching frequency on the efficiency, a further measurement was performed. The input voltage was set to U_{IN} = 200 V and the switching frequency was

increased from 9 kHz to 21 kHz, whereas all the other values and components were not changed. In Figure 5 it was found out that the efficiency is hardly affected by the switching frequency. As a conclusion it can be stated that the switching losses are significantly decreased and have a minor effect on the absolute losses. As reported in [1], the semi-conductor losses in the previous setup have a part of 60 % to 70 % of the total losses of the ZSI. With the new setup the switching losses are mostly eliminated so that the total losses of the ZSI are dominated by losses in other parts of the circuit e.g. chokes and filters.

The reduced switching losses allow the operation of the ZSI at a higher switching frequency without sacrificing efficiency. By doing so, the current ripple of i_Z and of the output current of the inverter is reduced. The benefit is that the inductors and capacitances can be optimized with a subsequent reduction of size and costs of the components. On the other hand, the quality of the output voltage and output currents will be increased. The amount of harmonics and ripple due to the switching will be reduced, a result that is appreciated for the use of the ZSI in standalone applications.
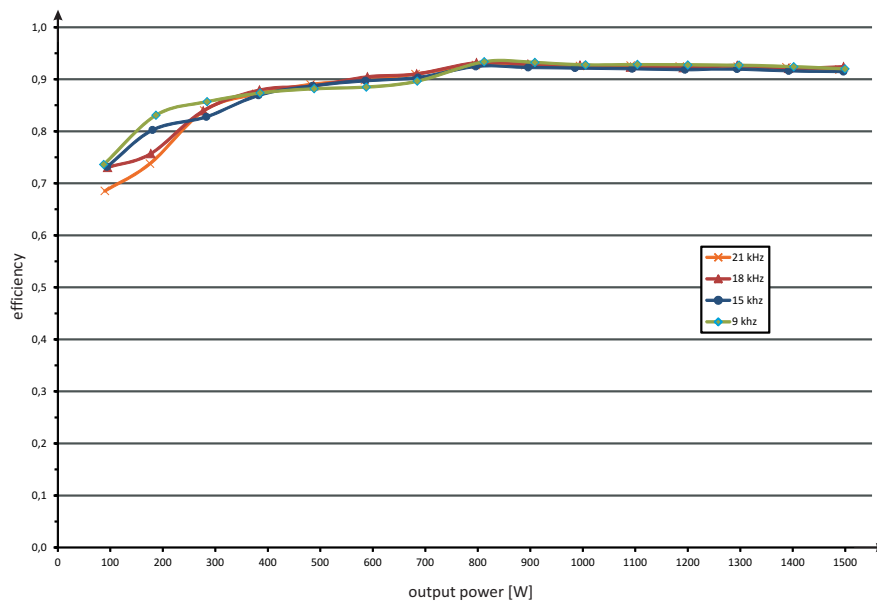

Figure 5: Influence of the switching frequency on the efficiency of the ZSI

6.   Further improvements in efficiency

As the losses in the semiconductors have been reduced significantly the balance of semiconductor losses and losses in passive components has changed. The losses occurring in passive components such as chokes and filters now have a higher influence in efficiency. Therefore, the main inductors and the inductance of the output filter were redesigned. The first set of inductors was not optimized und used only to verify the functionality of the setup. With the inverter operating at these unfavorable conditions a temperature increase of up to 30°K on the surface of the inductors could be measured. Therefore after the introduction of SiC switches and reduction of switching losses the task of reducing the total losses by redesigning the chokes was considered. Table 2 shows a comparison of some data of the old and the new design of the main inductance L_Z. As it was intended to increase the switching frequency the inductance was reduced. Even though the volume of the inductance was slightly reduced the new one is capable of handling more current. Ferrite cores are now used for the main inductances L_Z and the output inductance L_F. During operation the surface overtemperature of the new inductors remained much lower than in the old set-up which means that their losses have been reduced.

In a further step the overall efficiency of the set-up equipped with the improved set of inductors was determined. The input voltage was set to U_{IN} = 200 V and the switching frequency was changed to 21 kHz. The result can be seen in Figure 6. For the sake of comparison the bottommost curve shows the efficiency of the ZSI with the old first configuration i.e. equipped with Si semiconductors and with the first set of inductors and operated at 9 kHz. In the old set up the efficiency reaches a maximum value of only 87 %. As mentioned above in the next step the semiconductors where changed to SiC ones. This increases the maximum efficiency to 92 % (middle curve). In both cases the inverter is still operated at 9 kHz so no benefits in terms of voltage quality and inductor size. Yet the efficiency could be increased by at least another 2 % when using the new set of inductors (topmost curve). Even though the switching frequency is now changed to 21 kHz the efficiency can still be increased. The peak efficiency is raised to 95 %. With the new setup one can combine both higher efficiency and better voltage and current quality.
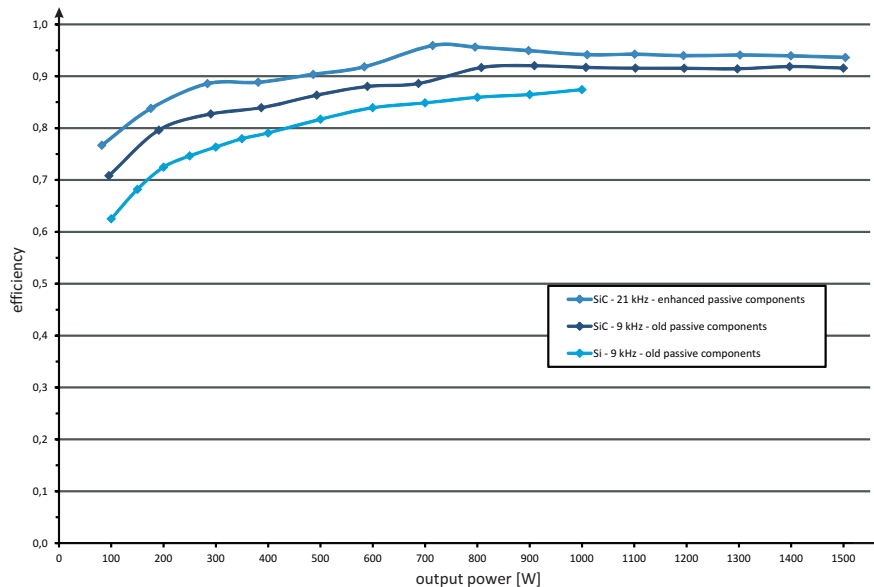

Figure 6: Overview of the efficiency improvements

7.   Conclusion

A ZSI that was developed for application in energy generation in the power range of some kWs is now optimized in order to increase its efficiency. With this objective two different actions were taken. The substitution of standard Si-IGBT with SiC ones clearly increases the efficiency of the system. Depending on load and input voltage level, the efficiency could be increased from 4 % to 6 %. When changing the switching frequency, the efficiency hardly changes. The semiconductor losses now barely influence the ZSI efficiency. In contrast to the Si-IGBT equipped setup, the passive losses now have the major part of the total losses. As a sub sequential step, the inductors where replaced as well. This gives another 2 % increase in efficiency achieving a peak efficiency of 95% and increasing the quality of the output voltage.

8.   References

[1] Mario Pacas, Manuel Steinbring, *Modified Control Structure for Single Phase Z-Source-Inverter and Efficiency Analysis,* PCIM 2012, May 2012
[2] Mario Pacas, Manuel Steinbring, Mohammed Allnajar, *Emulation of a Micro-Hydro-Turbine for*

Standalone Power Plants with Z-Source Inverter, IECON 2012, October 2012

[3] Fang Zheng Peng, *Z-Source-Inverter*, IEEE Transactions on industry applications, Vol. 39, No. 2, Mar./Apr. 2003

[4] Fang Zheng Peng, Miaosen Shen, Zhaoming Qian, *Maximum Boost Control of the Z-Source Inverter*, IEEE transactions on power electronics, Vol. 20, No. 4, July 2005

[5] T. Chandrashekhar, M. Veerachary, *Control of Single-Phase Z-source Inverter for a Grid Connected System*, Third International Conference on Power Systems, Kharagpur, INDIA, December 2009

[6] CENELEC standard voltages (IEC 60038:2009, modified); German version EN 60038:2011

9. Appendix

	old design	new design
nominal inductance	1 mH	0.55 mH
maximum current	16 A	30 A
DC resistance	32 mΩ	16 mΩ
Volumina	402 cm³	343 cm³

Table 2: comparison of the old and the new design of the main inductance L_Z