Resonant Circuit for the Reduction of the Power Pulsation in the DC-link of a Single Phase ZSI

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Abstract – **The present paper analyzes the reduction of the double frequent power pulsations in the DC-link of a single phase ZSI by using a passive resonant circuit. Three possible and effective topologies for the resonant circuit have been examined. The advantages and disadvantages of the three versions have been discussed in this paper and validated by measurements on a laboratory set-up.**

Index Terms **– power electronic converters, resonator filters, micro grids, Z-source inverter**

I. INTRODUCTION

The Z-source inverter (ZSI) has found to be a reliable and robust circuit capable of delivering a constant output voltage from a variable voltage input source. Due to its boosting capabilities, it can handle a wide range of input voltages either DC or AC. This makes it ideal to harvest energy from regenerative sources with a variable output voltage such as solar panels or hydro turbines. Thinking of outlying regions this power can be used to supply various electric home appliances. As the power rating is normally rather low, a single-phase output is used. A principal problem in single-phase systems is that the active power, which is delivered to the single-phase output is not constant, but pulsates with the double output frequency. In case of the ZSI this pulsation is passed through the whole system and causes an undesired component with this double frequency in the input current of the inverter. When using a three-phase generator to provide the input power, the pulsating current will cause an undesired torque ripple and an associated mechanical stress that should be avoided or at least reduced. The pulsation also causes higher losses and affects the stability of the control as well. Therefore, a LC series resonant circuit is used to absorb this oscillation in the ZSI. When tuning the resonant circuit exact to the right frequency, it can reduce the double frequent oscillation and enhance the whole system. This classical solution is applied to the ZVI and presented in the following with its advantages and drawbacks.

II. Z-SOURCE INVERTER

A. *Circuit Analyzis of the Z-source Inverter*

The topology of the analyzed ZVI without any resonant circuit is depicted in Fig. 1. The input voltage is supposed to be provided by a variable transformer connected to the grid. The resulting DC - voltage is smoothed by a capacitor C_{IN}.

For analyzing the ZSI, a symmetric design for the z-network is assumed. This means that both inductances and both capacitances have the same value.

$$L_{Z1} = L_{Z2} = L_Z \tag{1}$$

$$C_{Z1} = C_{Z2} = C_Z \tag{2}$$

When analyzing the ZSI generally two separate states within the switching period T are distinguished: The shoot through state in which one leg of the H-bridge is short circuited and is applied for the duration of T_S. The remaining time of the whole period T_1 is short circuit free and is available for standard PWM strategies. T_1 is again subdivided into an active part where the voltage $\hat{u}_Z$ is applied to the load and a freewheeling part where the output voltage of the H-bridge is zero. In this way the following duty cycles can be defined:

$$D_S = \frac{T_S}{T} \tag{3}$$

$$D_1 = \frac{T_1}{T} = \frac{T - T_S}{T} = 1 - D_S \tag{4}$$

The short circuit state of the output of the inverter can be analyzed by considering the change of the topology due to the shoot-through. The capacitors are now parallel to the inductances. U_{CZ} is the voltage over the capacitor C_Z that is at least loaded to the value of the input voltage U_{IN}. During shoot through state the voltage u_D becomes negative and the diode D blocks according to (5):

$$u_D = U_{IN} - 2U_{CZ} < 0 \tag{5}$$

$$u_{LZ} = U_{LC} \tag{6}$$

As a result, the current i_L through each inductance will rise. The output voltage of the inverter is zero in this state.

The remaining time is short circuit free and yield following equations:

$$u_{LZ} = U_{IN} - U_{CZ} \tag{7}$$

$$u_Z = U_{CZ} - u_{LZ} = 2U_{CZ} - U_{IN} \tag{8}$$

As the mean value of the voltage over the inductance must be zero, the voltage U_{CZ} can be calculated from (3) and (4) together with (6) and (7) as:

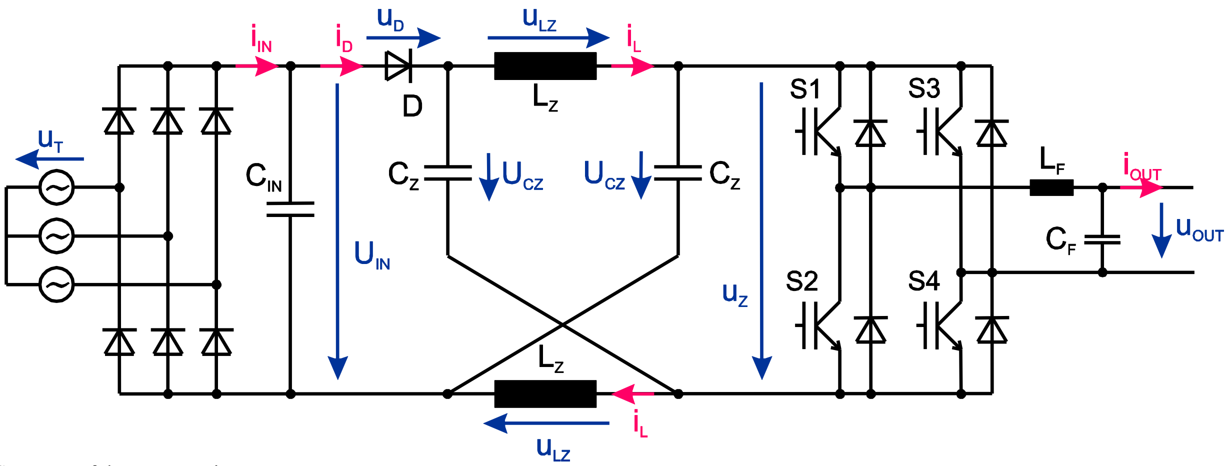

Fig. 1 Structure of the Z-source inverter

$$\bar{u}_{LZ} = \frac{T_S U_{CZ} + T_1(U_{IN} - U_{CZ})}{T} = 0$$
$$\Rightarrow U_{CZ} = \frac{T_1}{T_1 - T_S} \cdot U_{IN} = \frac{1 - D_S}{1 - 2D_S} \cdot U_{IN} \quad (9)$$

For the non-shoot-through state the voltage $\hat{u}_Z$ can be calculated by utilizing (8) and (9). u_Z is zero during the shoot-through and has its peak value during T_1. $\hat{u}_Z$ is also the value that is applied to the load through the H-bridge.

$$\hat{u}_Z = 2U_{CZ} - U_{IN} = \frac{T}{T_1 - T_S} \cdot U_{IN} = \frac{1}{1 - 2D_S} \cdot U_{IN} \quad (10)$$

This leads to the achieved voltage boost B, which is dependent on the shoot-through duty cycle D_S.

$$B = \frac{\hat{u}_Z}{U_{IN}} = \frac{T}{T_1 - T_S} = \frac{1}{1 - 2D_S} \geq 1 \quad (11)$$

Considering the modulation index of the PWM, the maximum boost factor of the ZSI is:

$$B_B = B \cdot M_{MAX} = \frac{1}{1 - 2D_S} \cdot (1 - D_S) \quad (12)$$

B. Control structure

For the single-phase ZSI a special control scheme is proposed which consists of two controllers as it is depicted in Fig. 2. In this scheme, the voltage control and the boosting are separated from each other. The first controller computes the boosting of the ZSI and the shoot through duty cycle D_S according to (12). First the reference value for the boost (shoot through) duty cycle D_S^* is calculated by dividing the required output voltage u_Z by the input voltage U_{IN}. The input voltage U_{IN} and the voltage U_{CZ} on the capacitor are used for the calculation of the actual D_S, which is compared with the set point value. The difference is fed into the PI-boost controller that corrects the shoot through duty cycle to the desired value. Thus, the simple open-loop calculation is improved.

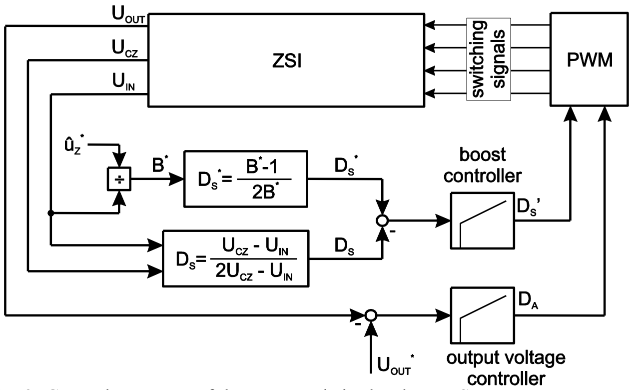

Fig. 2 Control structure of the proposed single-phase ZSI

In certain conditions the ZSI inverter operates in discontinuous conduction mode, in which the current through the inductor L_Z is not changing so the di_L/dt is zero and the voltage $\hat{u}_Z$ is less than expected. In the first stage of the experimental work, the control of the output voltage was realized without any feedback (open loop). Besides, the discontinuous mode was not detected. For these reasons, the output voltage could not reach the set point value. Under unfavorable conditions, the voltage U_{OUT} dropped to 190 V RMS. Therefore, an output voltage controller was introduced for the control of the active state duty cycle D_A and in this way of the output voltage. By using this control strategy, the output voltage can be kept constant at 230 V RMS regardless the conditions of the ZSI. The CENELEC grid requirements [2] can be fulfilled.

The outputs of the controllers deliver the values of D_S and D_A to the PWM that generates the switching signals. The calculated shooting time is applied as a negative dead time. By doing so, the shoot through can be easily included in the PWM-scheme and the number of switching transitions is not increased compared to standard voltage source inverter topologies.

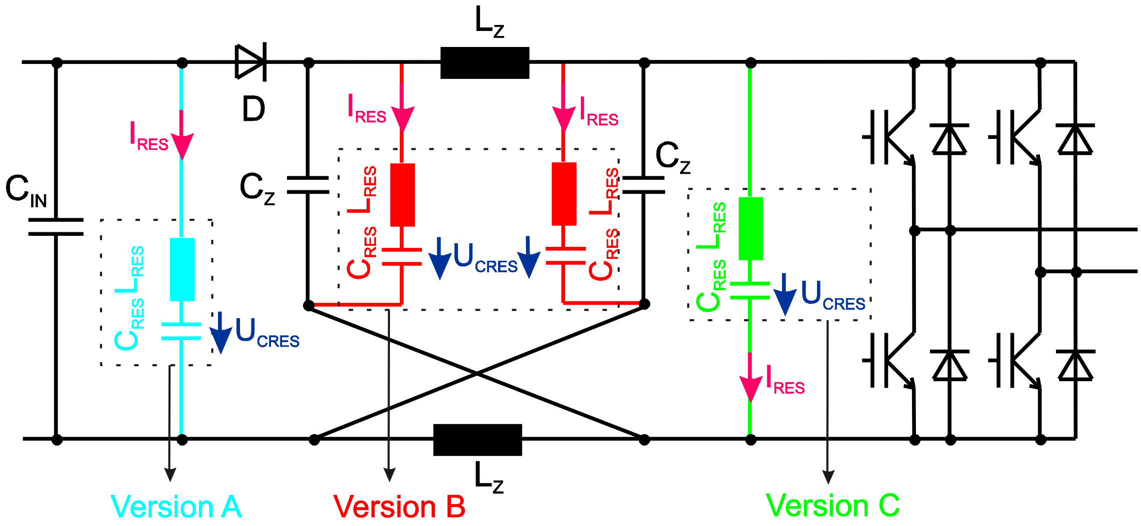

Fig. 3 Three different placement variations for the LC - resonant circuit

III. ZSI WITH ADDITIONAL LC RESONANT CIRCUIT

A principal problem in all single-phase inverters is that the output power is not constant. Moreover, it is delivered in a pulsating manner and normally this pulsation is passed through the whole system stressing all the components and the input source with the double output frequency. To avoid this energy has to be stored to balance out this pulsation. Therefore, a resonant circuit is added to a standard ZSI that balances out the pulsation appearing at 100 Hz.

The installation of a classical solution like the series resonant LC - circuit in a low-cost system for energy generation has to be carefully analyzed and has to take into account different constraints like: electrical and dynamic behavior, cost, volume, weight, impact on the whole efficiency and in case of the ZSI the most appropriate of the three possible topologies. Further interaction between the series resonant circuit and the ZSI might occur and cause malfunction to the inverter.

The first circuit variation results when the LC - resonant circuit is connected parallel to the input capacitor C_{IN}. In the second one each of two identical LC - circuits are connected parallel to each ZSI capacitor C_Z. As a third variation the LC - circuit is placed between the ZSI network and the H-bridge. These three different topologies can be seen in Fig. 3. They will be designated version A through C as they are labeled in Fig. 3. In all cases the resonant frequency of the filter is tuned to 100 Hz.

TABLE 1
VALUES OF THE MOST IMPORTANT INDUCTANCES AND CAPACITANCES IN THE ZSI SET-UP

L_Z	1,2mH
C_Z	100µF
C_{IN}	330µF
L_{RES}	14mH
C_{RES}	180µF

At first, simulations were performed comparing all three versions with the basic configuration without resonant circuit. The input voltage u_T was set to 160 V RMS thus the rectified input voltage U_{IN} is 220 V. This voltage is boosted so that a 230 V RMS sinusoidal output voltage U_{OUT} can be generated. The simulation was setup for an output power of 1.7 kW. Table 1 lists up important values of the simulated configuration.

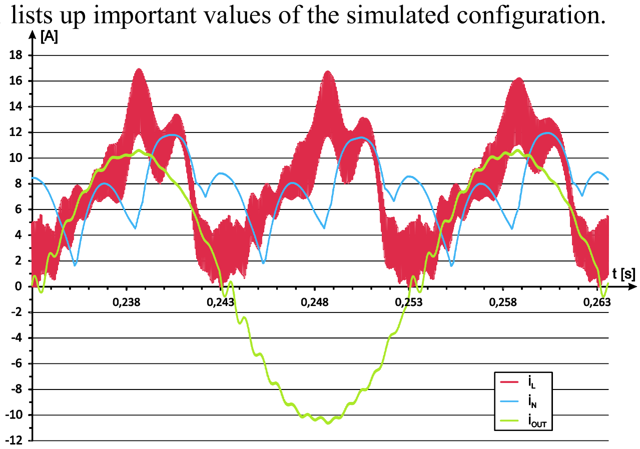

Fig. 4 Input current I_{IN} (blue), the current I_Z (red) and the output current I_{OUT} (green) of the ZSI without resonant circuit.

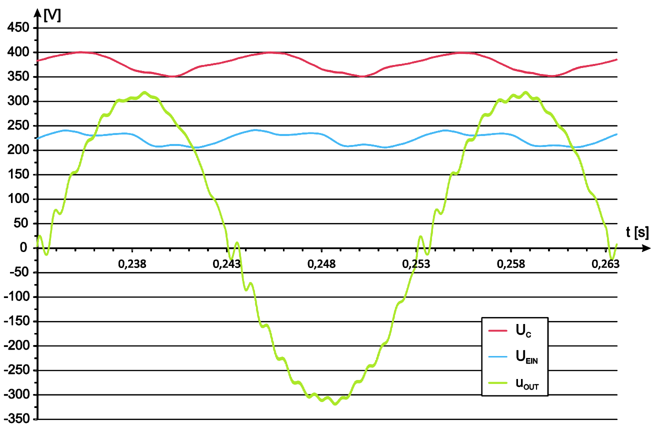

Fig. 5 U_{IN} (blue), U_{CZ} (red) and the output voltage U_{OUT} (green) of the basic ZSI without resonant circuit.

A. *Basic ZSI without resonant circuit*

For comparison, the ZSI without resonant circuit was simulated first. Fig. 4 shows the input current i_{IN} (blue), the current i_Z (red) and the output current i_{OUT} (green). The 300 Hz pulsation caused by the rectifier in i_{IN} and i_Z can be clearly seen. In the upper trace of Fig. 4 the 100 Hz pulsation that is caused by the single-phase output is also evident. The smallest value for i_{IN} is 2 A and the peak value is about 12 A. i_Z shows a similar behavior. The current varies between 0 and 17 A.

Fig. 5 shows the plot of U_{IN} (blue), U_{CZ} (red) and the output voltage U_{OUT} (green). Both U_{IN} and U_{CZ} are affected by a high pulsation. The peak-to-peak value of the AC component of U_{CZ} is 50 V. The inverter feeds a simple resistive and output voltage and current are proportional.

B. *Version A: LC - circuit parallel to C_{IN}*

In this configuration the resonant LC - circuit is parallel connected to the input capacitor. In Fig. 6 the same currents are shown as for the ZSI version without filter. Additionally the current i_{RES} through the resonant circuit is shown in purple. As expected, the current i_{RES} flowing through the resonant circuit is almost sinusoidal and has a 100 Hz frequency. It absorbs the energy pulsation and reduces the ripple of i_{IN}. The peak value of i_{IN} goes down to 12 A and the general waveform is enhanced, despite the 300 Hz pulsation due to the rectifier. Due to the position of the resonant LC – circuit in the whole topology, it does not affect i_{LZ} which still exhibits a high 100 Hz ripple. The peak value is even slightly higher than in the version without LC filter. The resonant current has an amplitude of 6 A. The output has not changed.

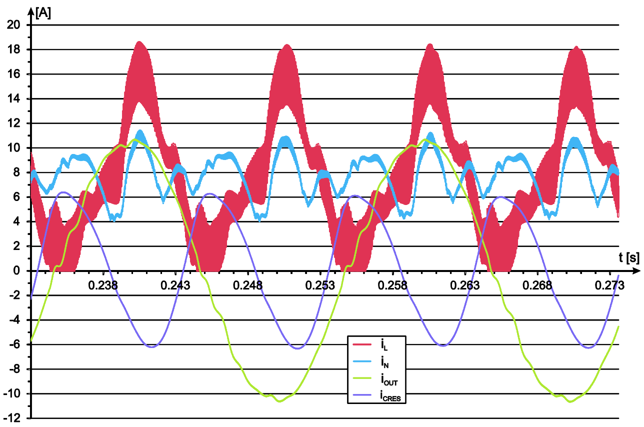

Fig. 6 Input current i_{IN} (blue), the current i_Z (red) the output current I_{OUT} (green) and the current through the resonant circuit i_{RES} (purple) of version A

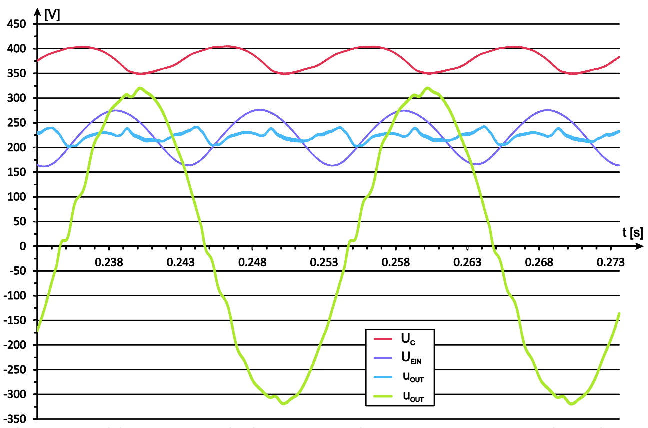

Fig. 7 U_{IN} (blue), U_{CZ} (red) the output voltage U_{OUT} (green) an the voltage U_{CRES} (purple) of version A

Fig. 7 shows the same voltages as in Fig. 5 and additionally the voltage U_{CRES} of the capacitor of the resonant circuit. The ripple of U_{IN} has been slightly reduced. U_{CZ} is not affected and still presents the 100 Hz pulsation. The voltage of the resonant circuit capacitor is a DC value with an additional AC component of 117 V peak-to-peak.

C. *Version B: LC - circuit parallel to C_Z*

For version B two identical LC - circuits are connected parallel to each C_Z. In this case, the design of the components of the resonant circuit is very important. The main capacitors C_Z have a substantial influence on the functionality of the ZSI. If their characteristic is overridden by the LC - circuit this might cause a malfunction of the ZSI. Therefore, a high value for L_{RES} has to be chosen. In this way, the capacitive behavior of the DC-link during shoot-through can be maintained.

Fig. 8 shows the same currents as in Fig. 4 with the same color code. Compared to Version A the peak value of i_{IN} is

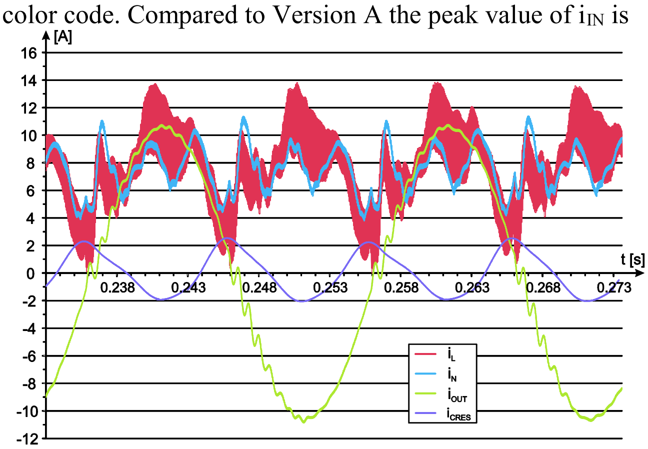

Fig. 8 Input current i_{IN} (blue), the current i_Z (red) the output current I_{OUT} (green) and the current through the resonant circuit i_{RES} (purple) of Version B

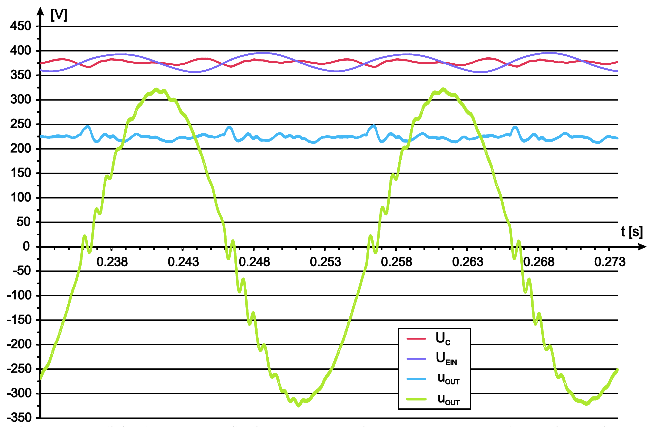

Fig. 9 U_{IN} (blue), U_{CZ} (red) the output voltage U_{OUT} (green) an the voltage U_{CRES} (purple) of version B slightly reduced but the general effect is similar. As the LC - filters are placed a closed to the output, the current i_L is now affected by the filters as well. The pulsation in i_L is smaller and its peak value becomes 14 A.

These results show that the currents through each filter have an amplitude of just 2 A. Two effects take place at this point. The filter stores a certain power for each period to balance out the pulsation. The demanded power is determined by the output power and is equal in all four versions. Compared to Version A this power can now be absorbed by two LC - circuits which reduce the required current to a half. Additionally they are operated at a higher voltage level compared to Version A, which also reduces the current.

This becomes evident when plotting the voltages as shown in Fig. 9. The voltage on the capacitor C_{RES} of the filter has a higher DC value and the AC part is smaller (39 V peak-to-peak). By applying the filters parallel to C_Z the quality of the voltage U_{CZ} is increased. The voltage ripple is reduced to 8 V. The AC component of U_{IN} is reduced significantly as well. The whole behavior of the system is smoother as the controllers are eased of the 100 Hz oscillations.

D. Version C: LC - circuit behind the ZSI network

In this version the LC - resonant circuit is placed between the characteristic LC network of the ZSI and the output H-bridge. At this position the LC - filter will be directly affected by the shoot through state of the ZSI and will be short circuited every switching period. Disturbances and malfunctions were therefore expected. Yet if the difference between the resonant frequency of the LC - filter and the switching frequency of the ZSI is large enough, the short circuit will not affect the resonant circuit. In the simulation, the switching period was 10 kHz which is 100 times higher than the resonant frequency of the filter. This worked well.

Analyzing the currents in Fig. 10 it can be seen that the input current i_{IN} has the best waveform compared to all other versions. Only a small 100 Hz pulsation is visible. The peak value is about 10 A. Compared to Version B the ripple of i_L could be reduced even more. The minimum value is not smaller than 2 A and the peak value is about 12 A. The peak value if i_{RES} is

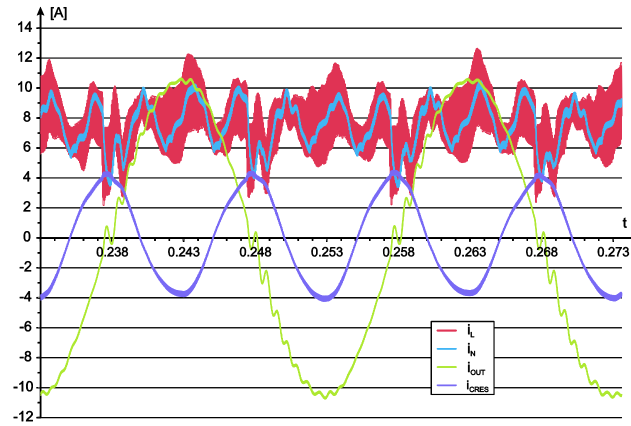

Fig. 10 Input current i_{IN} (blue), the current i_Z (red) the output current I_{OUT} (green) and the current through the resonant circuit i_{RES} (purple) of Version C

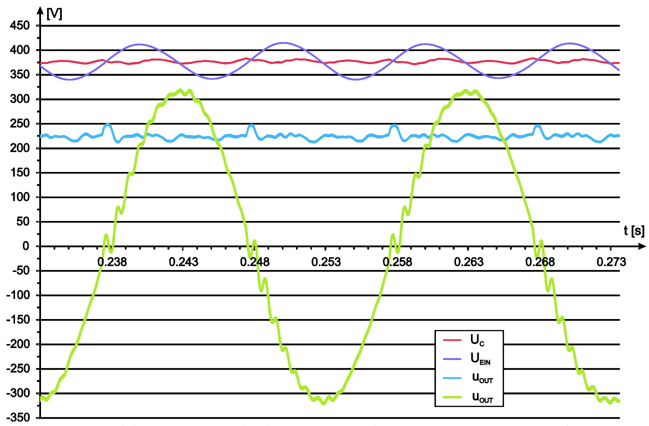

Fig. 11 U_{IN} (blue), U_{CZ} (red) the output voltage U_{OUT} (green) an the voltage U_{CRES} (purple) of version C

higher than in Version B but smaller than in Version A (4 A peak). That is because only one filter is used compared to Version B but it operates it at a higher voltage level compared to Version A.

The main capacitor voltage U_{CZ} is even smoother than in Version B, which had already excellent values (Fig. 11). The ripple of U_{IN} is similar good as in Version B. As only one filter is used the ripple of U_{CRES} is higher than in Version B (73 V peak to peak) in order to cope with the power demand.

E. Dimensioning the LC - resonant circuit

For dimensioning the resonant LC – circuit it is not only important to tune it to the right frequency. For doing so, there are many possible combinations of L and C that result into 100 Hz resonant frequency. In the design stage is important to avoid any disturbances in the function of the ZVI. As mentioned already it is important to choose a rather high value for the inductor. For the simulation study L_{RES} = 14 mH was chosen. Any higher value will work. Simulations were performed with a ten times smaller value of L_{RES} = 1.4 mH. The simulation results show that the system runs unstably. It takes more time to reach a stationary operation point. Additionally it is prone to high frequency oscillations. The filtering characteristic is reduced. As a conclusion it is better to choose a high value for L_{RES}.

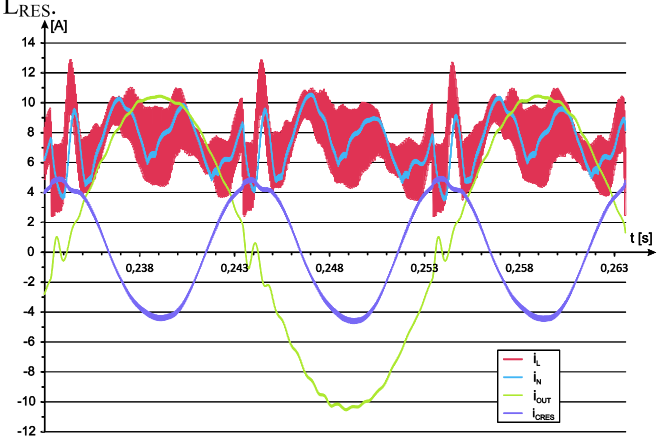

Fig. 12 Input current i_{IN} (blue), the current i_Z (red) the output current I_{OUT} (green) and the current through the resonant circuit i_{RES} (purple) of Version C when mistuning the resonant circuit to 90 Hz.

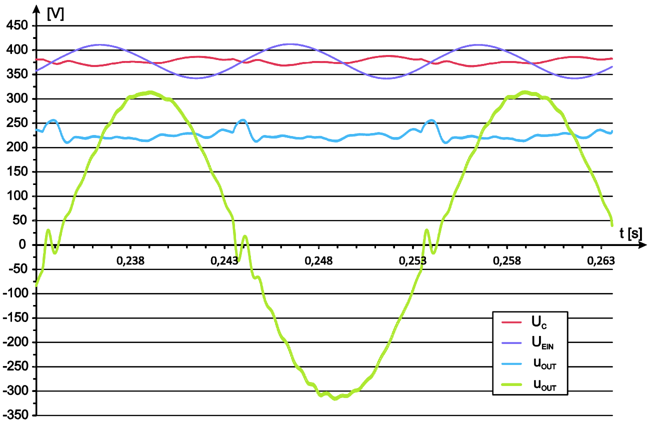

Fig. 13 U_{IN} (blue), U_{CZ} (red) the output voltage U_{OUT} (green) an the voltage U_{CRES} (purple) of version C when mistuning the resonant circuit to 90 Hz.

When it comes to practical implementation, it might not be possible to match the resonant frequency exactly as all devices have tolerances. Some of them may have variation of up to 20 % of its nominal value. The behavior of the ZSI was examined when the resonant circuit is mistuned by $\pm 10\text{Hz}$. Therefore the capacitor value in Version C was changed from 150 µF up to 220 µF (-17 %, +22 % of f_{RES}).

The simulation results can be seen in Fig. 12 and Fig. 13. The basic behavior is the same. The filtering effect still takes place. Comparing the mistuned with the correctly tuned version one can recognize that the filtering is not that effective anymore and the current through the filter is now distorted. Further, the voltage ripples are slightly higher. It can be concluded that a mistuning of the resonant circuit does not have a serious effect in the ZSI.

Summarizing the different placement variations. All three versions reduce the pulsation on the input current significantly and comply with the goal to free the input power source from the 100 Hz power pulsation. Version A is the least favorable version. The inductance of the LC - circuit has to be designed for the highest current and only the input current is affected. Version B and C give better results on a similar good level. Both versions reduce the ripple of i_{IN} and the i_Z as well and operate the resonant circuit on a higher voltage level. This allows one to reduce the size and cost of the inductors. The major tradeoff is using either two small resonant inductors or one bigger version. Version C was chosen to be investigated in further practical experiments.

IV. LABORATORY MEASUREMENTS

As version C showed the best results during simulation it was implemented and examined in practical tests. A MKV capacitor with a value of 137 µF was combined with an iron core inductance of 17.7 mH to reach a resonant frequency of 102 Hz. These values vary slightly from the simulated values. The value of 150 µF of the DC link capacitance C_Z was slightly higher than in simulation. The maximum load was only increased to 1250 W due to practical restrains.

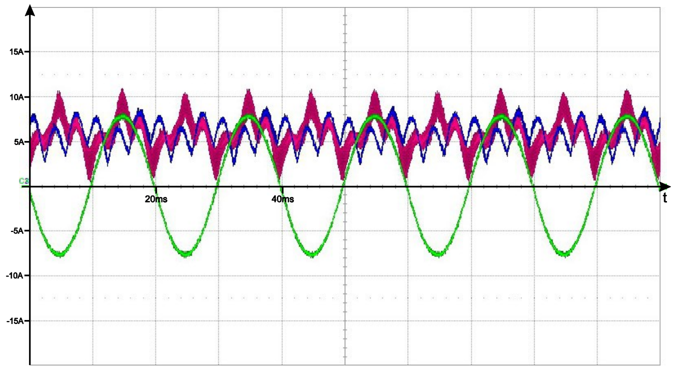

Fig. 14 Measurements showing the input current i_{IN} (blue), the current i_Z (red) the output current I_{OUT} (green) of the unmodified ZSI

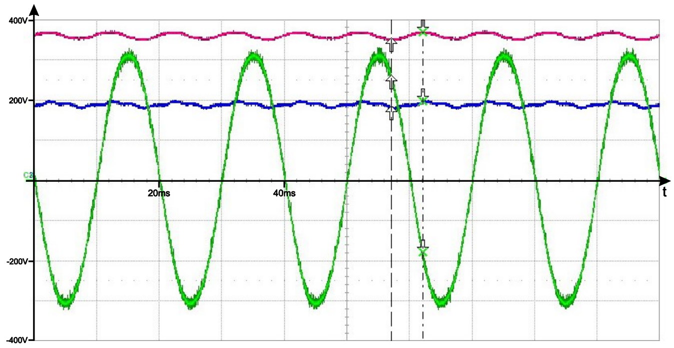

Fig. 15 Measurements showing U_{IN} (blue), U_{CZ} (red) the output voltage U_{OUT} (green) of the unmodified ZSI.

At first, measurements where performed with the unmodified ZSI. The results are shown in Fig 14 and Fig. 15. It can be seen that the 100 Hz pulsation is visible in all quantities, (except for the output values). Especially i_Z is prone to a significant pulsation. The peak value of i_Z is higher than 10 A. The AC part of the voltages U_{IN} and U_{CZ} have a peak-to-peak value of 23 V and 24 V. Comparing these results with the simulation results the pulsations are not as high. This can be explained by the previously mentioned differences.

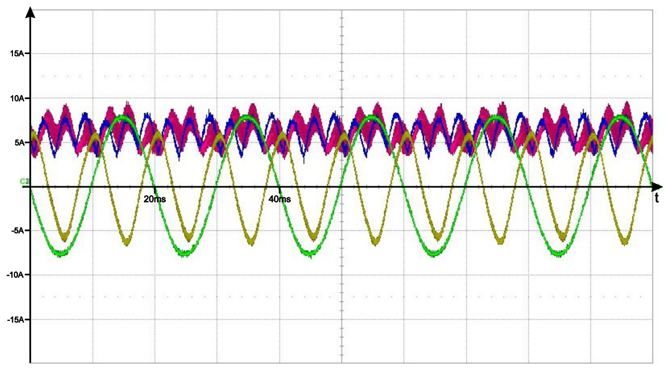

Fig. 16 Measurements showing the input current i_{IN} (blue), the current i_Z (red) the output current I_{OUT} (green) and the current through the resonant circuit i_{RES} (yellow) of Version C.

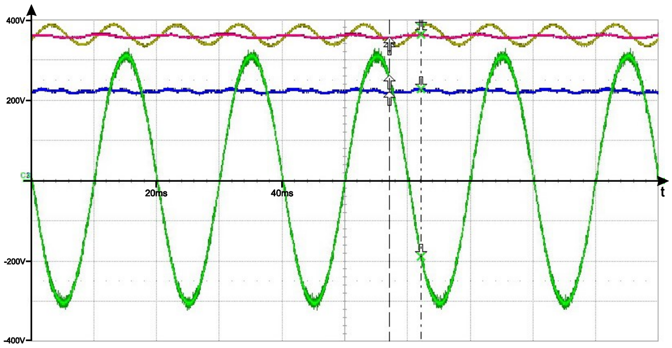

Fig. 17 Measurements showing U_{IN} (blue), U_{CZ} (red) the output voltage U_{OUT} (green) and the current through the resonant circuit i_{RES} (yellow) of Version C.

Fig 16 and Fig. 17 show the measurement when adding the resonant circuit at Position C. The effect of reducing the pulsation is mostly visible at i_Z. The peak is now reduced to below 10 A and the current shows a much more continuous current flow if the 300 Hz pulsation caused by the rectifier is ignored. This can also be recognized at the curve of i_{IN} that the 300 Hz pulses have nearly the same peak value. For the voltages it can be stated, that the AC component is reduced to 19 V for U_{IN} and 15 V for U_{CZ}. The curves of the output voltages and current do not change.

Comparing the results with the simulation it can be stated, that the filtering effect in laboratory is less visible. The laboratory work showed that the filtering effect of the resonant circuit is much more sensitive to mistuning of the filter and parasitic characteristics of the inductance and capacitance than it was in simulation. Besides the real behavior of the capacitors with their intrinsic resistances (that was not considered in the simulation) leads to a higher damping and to a reduction of the filtering effect.

The filter components result to be bulky und heavy. Even with an optimized inductance and higher quality capacitors they would still have a reasonable size and weight. This might be not a drawback in stationary systems but the overall cost is increased and a reduction of the losses is questionable and has to be analyzed.

It can be concluded that integrating a resonant filter to the ZSI reduces the pulsation that is caused by the single-phase load. The effort that is required to reduce the pulsation is rather high. Additional components add to losses and cost of the system. Therefore, it is easier and cheaper to just increase the input and DC link capacitances to reduce the pulsation. The use of an active filter is questionable as well because the number of components increases and in the availability of the system is affected.

V. CONCLUSION

This paper investigates the influence of a series resonant LC-circuit in the DC-link of a single-phase ZSI. The goal is to eliminate the 100 Hz pulsation of the input current that stresses the input source and in case of a generator produces undesired torque oscillations. This effect is inherent to the single-phase output that delivers the active power with a frequency of 100 Hz. Three different topologies for a resonant LC-circuit and their effect in the operation of the Z-source inverter have been examined. In Version A the circuit is connected parallel to C_{IN}, in version B two identical circuits are placed each parallel to one C_Z and in Version C the resonant circuit is placed between the Z-source network and the output H-bridge. All three versions reduce the ripple on the input current i_{IN} significantly and comply with our goal. Version B and C additionally reduce the ripple if the current i_L and are the favorable versions.

Laboratory measurements show that the ripple can be reduced by integrating a resonant filter to the ZSI. The drawback though is the size and cost of the additional components as well as their additional losses.

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