Modified Control Structure for Single Phase Z-Source Inverter and Efficiency Analysis

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Abstract

This paper introduces a modified control structure for controlling the boost factor of a single phase Z-Source inverter. In difference to other control methods, in which the capacitance voltage is controlled, the control of the inverters output voltage is proposed. The control scheme provides fast response to input voltage changes, simple implementation and high ruggedness. The method is proved on a laboratory implementation of the Z-Source inverter. Further, an efficiency analysis of the Z-Source inverter is accomplished by taking into consideration the variation of the input voltage.

Introduction

For generating power in outlying regions small regenerative energy sources like small hydro power plant or solar panels can be used. They can provide small amounts of energy for electric light, refrigerators or other applications. Taking the small hydro power plant as an example the output voltage highly varies with the available water flow. In order to provide a usable voltage-characteristic i.e. amplitude and frequency, the incoming energy has to be converted. In standard topologies the voltage is boosted in the first stage and is converted into the desired voltage in the second one. Typically a boost converter feeds a standard H-bridge in such applications. The Z-Source inverter (ZSI) provides this functionality in only one stage [1]. It can cope with a widely varying input voltage converting it directly into the desired voltage. In comparison with a standard voltage-source inverter (VSI) a shoot-through state of the output inverter is not just tolerated but an important part of the functioning principle. This feature makes the ZSI ideal for standalone power generation in outlying regions as it increases the ruggedness of the inverter. For those applications the utilized equipment should be cheap and robust and provide a high efficiency.

1 Circuit Analysis of the Z-Source Inverter

The utilized circuit can be seen in Fig. 1. In the experimental set-up the input voltage is provided by variable transformer feeding a rectifier. The resulting DC - voltage is smoothed by capacitor. For analyzing the ZSI, a symmetric design for the Z-network is assumed. This means that both inductances and both capacitances have the same value.

$$L_{z_1} = L_{z_2} = L_z$$
 (1)

$$C_{z_1} = C_{z_2} = C_z$$
 (2)

When analyzing the ZSI generally two separate states within the switching period T are distinguished. Short circuiting the inverters output by closing two switches of one leg of the H-bride leads to the shoot-through state which is applied for the duration of T_s . The remaining time T_1 is short circuit free and is available for standard PWM strategies. T_1 is again subdivided into an active part where the voltage \hat{u}_7 is applied to the load and a

(4)

freewheeling part where the output voltage of the H-bridge is zero. In this way the following duty cycles can be defined:

$$D_{\rm s} = \frac{T_{\rm s}}{T}$$
(3)



Fig. 1: Structure of the Z-Source inverter

When short circuiting the inverters output the topology is changed. The capacitors are now parallel to the inductances. Because U_{CZ} is at least loaded to the same value as the input voltage U_{IN} , the voltage u_D becomes negative and the diode D blocks:

$$u_{\rm D} = U_{\rm IN} - 2U_{\rm CZ} < 0$$
 (5)

$$u_{LZ} = U_{LC}$$
(6)

As a result, the current i through each inductance will rise. The output voltage of the inverter is zero in this state.

The remaining time is short circuit free and yield following equations:

$$u_{LZ} = U_{IN} - U_{CZ} \tag{7}$$

$$u_{z} = U_{CZ} - u_{LZ} = 2U_{CZ} - U_{IN}$$
(8)

As the mean voltage of the inductance must be zero, the voltage U_{cz} can be calculated from (3) and (4) together with (6) and (7) as:

$$\overline{u}_{LZ} = \frac{T_{S}U_{CZ} + T_{1}U_{IN} - U_{CZ}}{T} = 0 \Longrightarrow U_{CZ} = \frac{T_{1}}{T_{1} - T_{s}} \cdot U_{IN} = \frac{1 - D_{s}}{1 - 2D_{s}} \cdot U_{IN}$$
(9)

For the non-shoot-through state the voltage \hat{u}_z can be calculated by utilizing equations (8) and (9). u_7 is zero during shoot-through and equal to its peak value during T₁. \hat{u}_7 is also the value that is applied to the load through the H-bridge.

$$\hat{u}_{z} = 2U_{cz} - U_{IN} = \frac{T}{T_{1} - T_{s}} \cdot U_{IN} = \frac{1}{1 - 2D_{s}} \cdot U_{IN}$$
 (10)

This leads to the achieved voltage boost B, which is dependent of the shoot-through duty cycle D_S.

$$B = \frac{\hat{u}_{Z}}{U_{IN}} = \frac{T}{T_{1} - T_{S}} = \frac{1}{1 - 2D_{S}} \ge 1$$
(11)

Considering the modulation index of the PWM, the maximum voltage boost of the ZSI is given by:

$$B_{B} = B \cdot M_{MAX} = \frac{1}{1 - 2D_{S}} \cdot (1 - D_{S})$$
(12)

2 Control structure

For the proposed control structure the voltages U_{IN} and U_{CZ} must be measured. A current measurement is not required, although it is measured and used for detecting inverter failures. In most control schemes U_{CZ} is regulated [5]. Here the peak output voltage \hat{u}_z is controlled. \hat{u}_z is the voltage at the input of the H-bridge during T_1 , so it determines the modulation index M for the PWM.



Fig. 2: Control scheme for a single phase Z-Source inverter

As seen in Fig. 2 the desired boost factor B* is calculated by using the measured value of U_{IN} and the value of \hat{u}_{z}^{*} that should be achieved. Rearranging (11) leads to a set point value for the shoot-through duty cycle D_{s}^{*} . This value could be directly applied to the PWM, but unfortunately real voltage values differ from the desired ones due to finite switching times, inverter dead times and other non-linearities. Therefore the actual shoot-through duty cycle is calculated by utilizing U_{IN} , U_{CZ} and (9). A PI-controller is used for the calculation of the PWM in a way that the difference $D_{s}^{*} - D_{s}$ is controlled to zero. The equations (11) (12) describing the ZSI maintain valid and \hat{u}_{z} can be directly used for modulating u_{OUT} . In order to reduce voltage stress and losses, the set point value of \hat{u}_{z}^{*} is changed according to the input voltage. As can be seen in (12) the shoot-through duty cycle must be changed inversely proportional to U_{IN} .

The H-bridge is basically driven by alternate switching. In standard VSI a dead time is required to prevent short circuits in the H-bride. Since a short circuit is part of the function principle no dead time is required. Therefore the dead time is replaced by the shoot-through state practical applying a negative dead time. In this way the amount of switching actions in comparison to standard switching patterns is not increased.

3 Experimental Results

Table 1 lists up some important parameters of the utilized self-designed ZSI which can be seen in Fig. 3. The variable three phase input AC voltage is converted into a DC voltage by a rectifier.

rated output power	1 kW
output voltage	230 V, 50 Hz AC
inductance L _z	600 µH
capacitor C _Z	470 μF
switching frequency	36 kHz

Table 1: Parameters of the experimental setup



Fig. 3: The utilized self – design ZSI. The dsPIC microcontroller can be seen on the board on the left of the picture. It is connected to the main board which contains the actual ZSI, gate drivers, measurement and power supply circuits. The Z-Source inductors are shown at the top of the picture.

Fig. 4 shows the voltages U_{IN} , U_{CZ} and u_Z and the current i_L for different input voltage levels. It can be seen, that \hat{u}_Z is being increased as U_{IN} decreases. The capacitor voltage remains constant. The input voltage varies from 150 V to 300 V. The load current i_{out}_{eff} is 4 A, which corresponds to a load of 920 W. For $U_{IN} = 150$ V (upper part of Fig. 4) a boost factor of B = 2.1 is required resulting in a D_S of 0.26.The ratio $\frac{u_{out}}{u_T}$ corresponds to a total voltage

boost factor of 3.6.

Another advantage of adjusting \hat{u}_z according to U_{IN} is the reduced current ripple of the inductor current which reduces discontinuous mode operation. During $T_s u_{LZ}$ is equal to U_{CZ} which is independent of the input voltage so that the rising edge of i_L has the same slope for different U_{IN} . In comparison the decreasing rate of i_L is being reduced with smaller U_{IN} as it is calculated according to (7). For $T_1 \hat{u}_Z$ can be calculated by

$$\hat{u}_{z} = U_{cz} - u_{Lz} = U_{cz} - L \frac{di}{dt}$$
 (13)

As soon as i_L falls to zero, the derivative part of (13) becomes zero as well. \hat{u}_Z has now a smaller value than expected. This results in a smaller voltage time integral of U_{OUT} and as a consequence a smaller amplitude of U_{OUT} . Therefore \hat{u}_Z is decreased as U_{IN} increases so that discontinuous operation can be reduced as far as possible. By increasing the value of L_Z the borderline to discontinuous mode can be pushed farther to no-load, but cannot be eliminated completely.



Fig. 4: u_Z , u_{CZ} , u_{IN} , i_L for two different input voltages. top: U_{IN} = 150V; bottom: U_{IN} = 300V

4 Efficiency analysis in relationship to input voltage

For analyzing the Z-Source inverters efficiency the output load is varied between no-load and 100 % of rated output power. To analyze the influence of the input voltage, this is done by changing U_{IN} . The input power is measured at the input of the rectifier by utilizing a wideband power analyzer. The output power is measured by using a power meter which measures u_{OUT} and i_{OUT} . This gives the overall efficiency of the circuit. The results of the measurement can be seen in Fig. 5.

If the input voltage U_{IN} is higher than the peak output voltage, the ZSI operates in normal inverter mode, no boosting is required. When $U_{IN} = 300$ V the ZSI provides an efficiency of up to 90 %. As the input voltage drops, the current consumption increases in order to reach the desired output power. This results in a decreasing efficiency level at smaller U_{IN} . If the input voltage drops to 150 V the efficiency reaches a maximum of 67 %.





In order to analyze the power losses and to increase efficiency some investigations have been done. As the diode D is the only further semiconductor in ZSI topology compared to standard VSI it was especially considered. For the operation of the ZSI this diode is very important as it disconnects the Z-Source network from the input during shoot-through so the boosting can be done. In the proposed setup it has to withstand high voltages. During shoot-through u_D can go up to 550 V when the input voltage U_{IN} drops to 150 V. Besides it has to conduct high currents during none shoot-through. If the input power goes up to 1500 W at U_{IN} = 150 V the current will go up to 10 A. The input diode was therefore replaced by a SiC - Diode. As it has almost no tail recovery current, the efficiency should increase. The measurement is done at an input voltage of 200 V and at changing load. The results can be seen in Fig. 6.



Fig. 6: Efficiency of the ZSI with conventional Si and SiC - Diode.

Fig. 6 shows that changing the diode does not have a big influence on the inverter's efficiency. The difference lies between 0 % and 2 %. Even though the diode is stressed much it is not having a big impact concerning the efficiency. The results can be confirmed by using further diodes.

In order to improve the efficiency in further work, it is investigated how the losses split up in losses that occur in the semiconductors and losses that appear somewhere else in the setup e.g. losses in inductors. To determine the losses produced by the semiconductors the temperature rise of the heat sink can be measured. To do this a reference measurement has to be done at first. A part of the power loss is caused in the semiconductors by driving a high current through the reverse diodes of the inverter. The temperature rise of the heat sink compared to ambient temperature is measured and correlated to the power loss. To determine the power losses in normal operation the temperature rise can be associated backwards to the power loss. As all semiconductors are mounted to one big heat sink the power loss of all semiconductors of the circuit can be determined. Fig. 7 shows the result. It can be seen, that the total losses increase as the output load increases due to higher currents. The relative power losses of the semiconductors results to be 60 % - 70%.



Fig. 7: Power losses separated into losses occurring in the semiconductors and in the passive components

5 Conclusion

This paper introduces a new control method for controlling the boost factor of the single phase ZSI. It is suitable for a wide input voltage range, stable and easy to implement which is proven by a laboratory setup equipped with a simple microcontroller. The efficiency analysis shows that the efficiency of the single phase ZSI decreases as the input voltage drops. The blocking diode at the inverters input only has a minor effect to efficiency. It can be shown that the losses generated by the semiconductors have a rate of 60 % – 70 % of total losses in the utilized setup.

6 Reference

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