Hardware Implementation of Balance Control for Three-Phase Grid Connection 5-Level Cascaded H-Bridge Converter using DSP

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Abstract— The objective of this paper is the implementation of a three phase 5-level cascaded H-bridge inverter connected to the grid. A voltage oriented control (VOC) based on space vector pulse width modulation technique (SV-PWM) is used for the control of the converter by using only a single DSP. A feedforward modulation index compensation is applied to overcome the problem of voltage imbalance among the different phases. Simulation and experimental results of a system with a 5-level CHB (Cascaded H-Bridge) inverter and grid connection are presented to validate the proposed topology and control method.

Keywords-Cascaded H-bridge; Multilevel inverters; photovoltaic (PV) power; systems, power conversion

I. INTRODUCTION

Grid connected photovoltaic energy conversion systems have been increasing in recent years due to the continuous reduction of the PV modules costs and the increase of the conversion efficiency as well as the rise in prices of fossil fuels. This trend is expected to continue in the coming years [1], [2].

As the power level of the PV systems increases and the grid connections are also installed at medium voltages, the system can benefit from the utilization of a multilevel converter because it represents an efficient solution for high power and medium voltage applications. It allows operating at voltage levels higher than the limits of the individual power switches in the conversion process. Moreover it can generate high quality currents and voltages with reduced common mode voltages and smaller voltage changes as well as the generation of lower EMI with reduced switching frequency and with higher efficiency [3].

The cascaded H-Bridge (CHB) multi-level converter topology has been widely proposed for PV conversion applications [1], [2], [4], [5], [7] - [14] because it offers a modular solution by collecting large numbers of PV panels as an isolated DC sources which allow to generate a large number of voltage levels in the output. These combinations achieve an individual maximum power point tracking (MPPT) through DC-DC converters improving the conversion efficiency of the system. CHB topology has some other advantages such as flexible design, easy installation and it requires a minimum number of components when compared to other multilevel inverter topologies with the same number of levels. One of the requirements in the CHB is the isolation between the PV sources at each cell of H-bridge, in order to prevent high voltages at the PV modules and the leakage currents generated by the parasitic capacitance of the panel under variable H-bridge voltages due to the modulation of the converter. Thus a cascaded inverter is one of the best topologies for high voltage grid-connected photovoltaic systems [1], [2], [4].

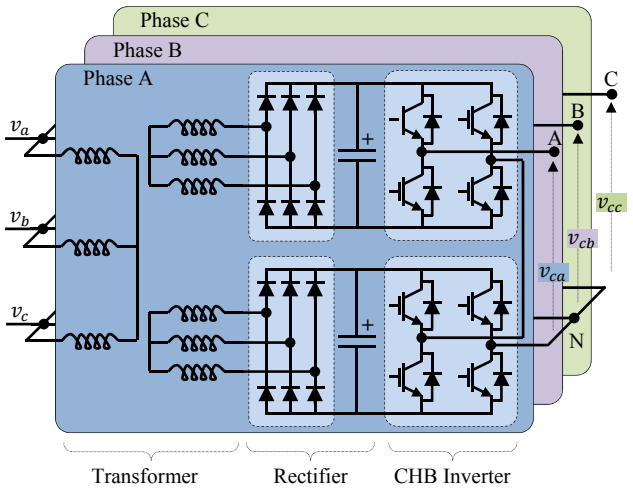

Fig. 1: Proposed system configuration of the 5 level CHB grid connection converter

However, this advantage comes along with drawbacks, which are the inherent power imbalance between cells in each leg as well as a power imbalance among the different phases of the inverter caused by dust accumulation, partial shading and module mismatch of the array [5].

Many reports can be found in literatures, which were carried out for solving these problems [2], [5] - [8], [14]. In [4] a simple feedforward mechanism was added to the control scheme as compensation to overcome the imbalance in DC-link capacitors voltages but unfortunately no laboratory results were presented for the validation of this solution. In [2], two types of power compensation methods

were proposed: one was to compensate the occurrence of imbalance among different cells in the same phase and the other was to compensate the power imbalance among the phases, here also, no laboratory results were shown either. In [5], the results of simulations proved that both types of power imbalance in the CHB were eliminated by connecting the whole PV generated power to a single dc-bus bar and a traditional Voltage Oriented Control was used for the grid tie CHB inverter to control the grid currents and dc-bus bar voltage without the need of any balancing algorithm.

This paper presents an implementation of a three phase 5-level cascaded inverter connected to the grid with voltage imbalance control using a single DSP. The control scheme is simple and was realized based on voltage oriented control (VOC) similar to the schemes reported in [2], [4]. A powerful space vector pulse width modulation technique (SV-PWM) is used to control the switching states of the inverter and a simple feedforward control is used to overcome the problem of voltage imbalance among the different phases in order to improve the system efficiency.

The paper is organized in the following way. Section II covers the description of proposed topology. Section III presents the control method of the converter system as well as the modulation strategy of the 5-Level CHB converter. Section IV provides simulation and laboratory results for the proposed system. Finally, section V summarizes the conclusions of the paper and gives an outlook on the ongoing projects.

II. PROPOSED TOPOLOGY

The proposed three-phase CHB 5-level grid connection system configuration is illustrated in Fig. 1. From the power circuit three main parts can be recognized: the H-bridge power cells of the CHB, the DC-link, and the isolation transformer. The proposal is based on the system presented in [2], [7] but the PV panel stage has been replaced by emulated PV stage using a transformer, a rectifier and capacitor filter combination in each cell. The CHB converter consists of a series of identical H-bridge cells, as shown in Fig. 1. Each H-bridge generates three output voltage levels. The series connection of the cells generates the output voltage waveforms that are synthesized by the combination of each output of the cells at certain switching state. In general, when k H-bridges are connected in series, the output waveforms contains n=2k+1 voltage levels. In this work, two cascaded H-bridges per phase generate a five-level phase voltage waveform at each phase of the converter. An inductive filter is used for connection of the converter to the grid and a transformer is used as an optional for isolation issues.

III. MODULATION AND CONTROL STRATEGY

Within a research study dedicated to the investigation of power electronics for renewable energy sources, different applications of this topology are examined. In a first step, the phase voltage imbalance issue caused by e.g. dust accumulation, partial shading and module mismatch of the array is solved by using Voltage Oriented Control (VOC), with the help of simple feed-forward modulation index compensation. The proposed scheme takes up the idea proposed in [15] - [17]. The principle of the proposed method takes advantage of the star connection of the CHB converter modules with floating star-point, which is not connected to the neutral of the grid. The star-point can be shifted away from the grid neutral, in order to keep balance line to line voltages which lead to balance line currents injected to the grid even though the inverter phase voltages are not balanced. It is important to emphasize that the scheme in this work will not perform any power distribution between the cells of the converter. This task will be approached in the future work.

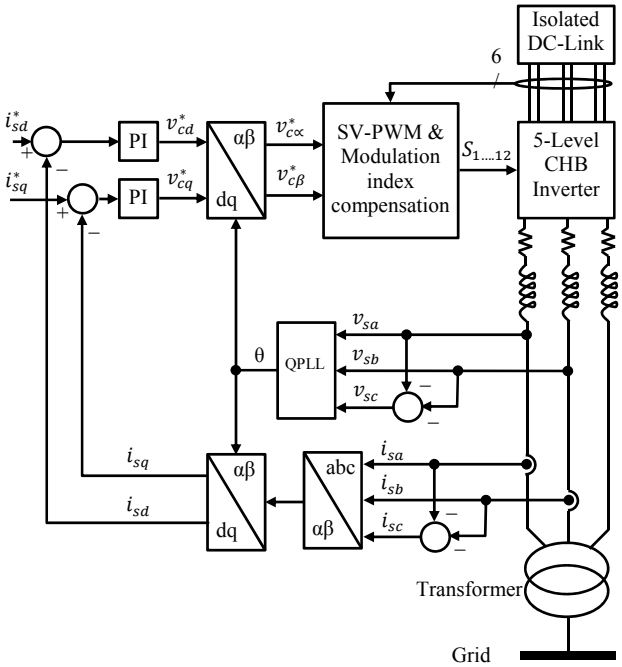

Fig. 2: Control diagram for the CHB converter system

A. Voltage Oriented Control (VOC)

The main task of the grid-tie inverter is to control active and reactive power injected to the grid. Voltage oriented control (VOC) is one of the most commonly control technique used for grid connection of converters which is used to regulate the interaction between the CHB and the utility grid. VOC scheme uses a rotating dq reference frame oriented with the grid voltage space phasor. All quantities are transformed from the natural abc-system to dc-quantities in the dq coordinates to simplify control system design. For this effect the well-known transformation is used:

$$\begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \cdot \begin{bmatrix} f_a \\ f_b \\ f_c \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} f_d \\ f_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \cdot \begin{bmatrix} f_\alpha \\ f_\beta \end{bmatrix} \quad (2)$$

The block diagram of the CHB with VOC is depicted in Fig. 2. In the dq reference frame, the real part of grid current

on the d-axis (i^*_{sd}) is proportional to active power and the imaginary part on the q-axis (i^*_{sq}) is proportional to the reactive power. The i^*_{sd} part of the reference current is adjusted manually while the i^*_{sq} part is set to zero in order to inject the energy to the grid with unity power factor. The *dq* currents are controlled using PI-controllers, whose outputs are the *dq* reference voltages (v^*_{cd} and v^*_{cq}). These are converted to αβ values ($v^*_{c\,\alpha}$ and $v^*_{c\,\beta}$) to be compensated then by DC-link feedforward and modulated by the CHB inverter using SV-PWM. The synchronization of the *dq* transformation is performed using a Phase Locked Loop (PLL) in order to have the *dq* frame correctly aligned with the grid voltage space phasor, the grid phase voltages are measured (v_{sa} and v_{sb}) for this issue. Finally the loop is closed by using the current measurements in which the phase currents i_{sa} and i_{sb} are measured (the third one i_{sc} is calculated internally) and transformed to αβ first, and then to *dq* values (i_{sd} and i_{sq}).

The equations governing control are as follows:

$$v_{ca} = v_{sa} + R_s i_{sa} + L_s \frac{di_{sa}}{dt} + v_{Nn} \tag{3}$$

$$v_{cb} = v_{sb} + R_s i_{sb} + L_s \frac{di_{sb}}{dt} + v_{Nn} \tag{4}$$

$$v_{cc} = v_{sc} + R_s i_{sc} + L_s \frac{di_{sc}}{dt} + v_{Nn} \tag{5}$$

where R_s is an inductive filter resistance, L_s is an inductive filter inductance, v_{Nn} is the voltage difference between inverter (v_N) and grid (v_n) neutral points which is equal to zero under balance conditions.

B. Feedforward compensation

Fig. 3 shows the feedforward compensation scheme according to the following equations:

$$V_{DC} = \frac{V_{DCa} + V_{DCb} + V_{DCc}}{3} \tag{6}$$

$$v^{**}_{ca} = v^*_{ca} . \left(2 - \frac{V_{DCa}}{V_{DC}}\right) . k_p \tag{7}$$

$$v^{**}_{cb} = v^*_{cb} . \left(2 - \frac{V_{DCb}}{V_{DC}}\right) . k_p \tag{8}$$

$$v^{**}_{cc} = v^*_{cc} . \left(2 - \frac{V_{DCc}}{V_{DC}}\right) . k_p \tag{9}$$

where V_{DCa} , V_{DCb} and V_{DCc} are the sum of DC-link voltage of two cascaded cells of phase *a*, *b* and *c* respectively. V_{DC} is the average sum of the total inverter DC-links voltages. k_p is the gain of P-controller.

The reference voltages in stationary reference frames $v^*_{c\,\alpha}$ and $v^*_{c\,\beta}$ obtained from the PI-controller are converted to *abc* reference frame as:

$$\begin{bmatrix} v^*_{c\propto} \\ v^*_{c\beta} \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} . \begin{bmatrix} v^*_{cd} \\ v^*_{cq} \end{bmatrix} \tag{10}$$

$$\begin{bmatrix} v^*_{ca} \\ v^*_{cb} \\ v^*_{cc} \end{bmatrix} = \begin{bmatrix} 1 & 1 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} . \begin{bmatrix} v^*_{c\propto} \\ v^*_{c\beta} \end{bmatrix} \tag{11}$$

For simplicity the phase *a* is taken for explaining the mechanism of compensation. The DC-link voltage V_{DCa}(sum of two cell DC-link voltages in the same phase) is normalized dividing by the total average DC-link voltage V_{DC} (average sum of six cell DC-link voltages) to have a per unit ratio of the voltage drift. This is subtracted from 2 per unit to compute the per unit error. This error is controlled using a P-controller. Then the correcting control signal is used to compensate the modulation index v^*_{ca}, and obtain the new phase output voltage reference v^{**}_{ca}. Afterward the compensated controlled voltages in *abc* reference frame are converted again to the stationary reference frame $v^{**}_{c\,\alpha}$ and $v^{**}_{c\,\beta}$

$$\begin{bmatrix} v^{**}_{c\alpha} \\ v^{**}_{c\beta} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} . \begin{bmatrix} v^{**}_{ca} \\ v^{**}_{cb} \\ v^{**}_{cc} \end{bmatrix} \tag{12}$$

and sent to the modulation stage, which is the same, i.e., SV-PWM.

C. Space vector modulation (SV-PWM)

Space vector PWM has several attractive features. It is suitable for digital implementation, has great flexibility in switching pattern design, etc. However, the high number of degrees of freedom in multi-level inverters with more than three levels makes the implementation of a space vector modulation algorithm difficult. A five-level CHB converter has six H-bridge cells with two cell per phase. Each cell has two legs of identical power switches (IGBTs) and each leg is controlled with two switching signals. The total switching signals are 12, so that the converter has $2^{12} = 4096$ switching combinations that will generate 125 different states in the converter output. Hence the SV-PWM algorithm is associated with very high computational effort due to high number of space vectors and of redundant switching states. Various researchers [18] - [24] have developed a wide range of PWM algorithms in order to reduce the computational effort. In this work, the modulation strategy is performed based on the technique presented in [18] in which a cycle of modulation is performed in three steps: the first step consists of the selection of nearest three space vectors to the reference vector and of the calculation of the on-times. A linear transformation has been used to simplify and speed up the mathematical calculation. The second step is the generation of the states corresponding to the selected space vectors and the determination of the sequence in which the minimum common mode voltage and the minimum number of switching transitions are achieved. The last step is the generation of the firing pulses by building a state machine in order to distribute the switching actions evenly between the power semiconductors. More details about 5-Level SV-PWM can be found in [18].

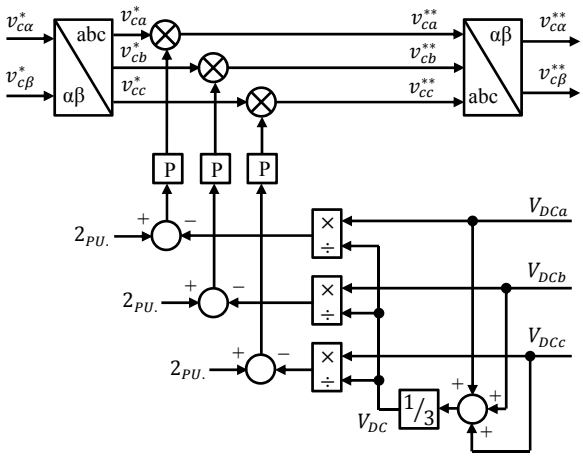

Fig. 3: Feedforward modulation index compensation diagram

IV. Simulation and Experimental Results

The performance of the 5-level CHB grid connected inverter under conditions of imbalance has been evaluated based on a MATLAB/Simulink environment as well as in laboratory setup. In Simulink, the modulator, the controller and the overall grid-connection necessary code are written in C code using the system function of MATLAB. The same code is used to program the DSP card in hardware.

Normally, a DSP platform is used to handle a part of the SV-PWM algorithm and an external logic unit such as FPGA is used to perform the rest of the modulation cycle which is a determination of the switching state of each H-bridge according to the selected phase potentials [18]. In this work, the complete modulation cycle was performed using only a single DSP.

An experimental five-level three-phase modular cascaded converter, shown in Fig. 4, was constructed using six identical H-bridge modules (two H-bridge per phase). Each H-bridge was built in a single board containing four discrete IGBTs of type IRGPH40UD. Each isolated DC-link was produced using a 50-Hz isolation transformer and a three-phase rectifier, while the overall cascaded converter switched output was connected to the 50-Hz grid via an inductive filter. The system is controlled by a floating-point digital signal processor unit based on TMS320F28335 eZdsp. This board is especially devised for control tasks and includes 12-bit sixteen independent A/D converters. The same C code used in Simulink is compiled to machine language using code composer studio v3.3 and is downloaded to the DSP. The communication between the DSP board and the computer was carried out by using the standard USB interface. Fiber optic communication interface is used in order to avoid the influence of noise in the firing pulses.

The results of voltages and currents waveforms are presented in Fig. 5-12. The currents and voltages are expressed in per unit being on the primary side of the transformer (1pu = 120 V, 1pu = 15 A). The steady state and dynamic behavior of the system under normal conditions (no voltage drift in the DC-links) for both simulation and laboratory are presented first and the behavior of 50% voltage drift in one cell in phase a is presented next.

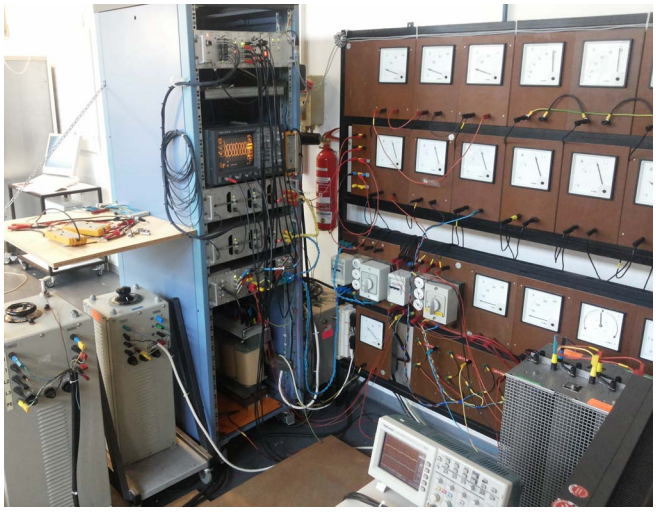

Fig. 4. Laboratory setup

A. Normal condition (equal DC-link voltages)

The total inverter output phase voltages are shown in Fig. 5, in which the inverter currents are shown in Fig. 6.

Fig. 7 shows the grid voltage and inverter current in phase *a*. They are completely in phase, and the grid current is almost sinusoidal with low ripple.

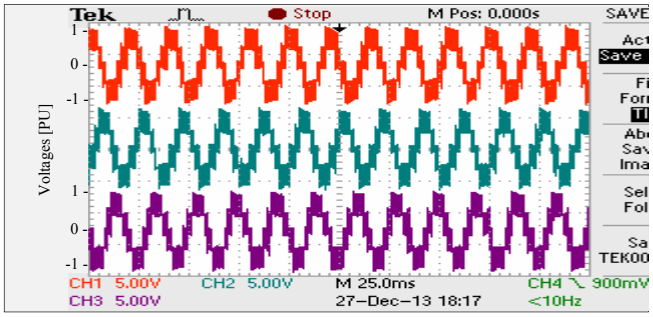

Fig. 5. Total inverter phase voltages under normal condition (25 ms/div)

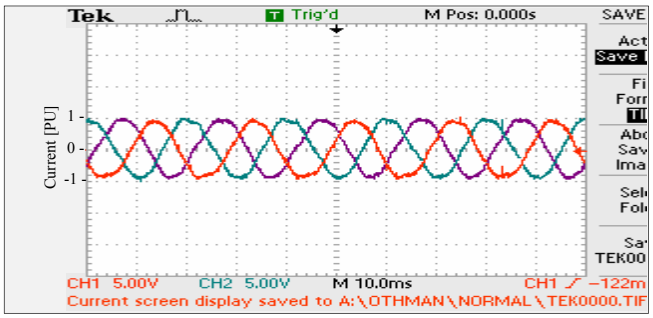

Fig. 6. Inverter currents enjected to the grid under normal conditions (10 ms/div)

The behavior of the controller is shown in Fig. 8, in which the inverter current i_{sd} tracks a 50% step change in the

reference current i_{sd}^{*} with zero steady state error, and Fig. 9 presents the behavior of the balanced currents injected to the grid under this step change.

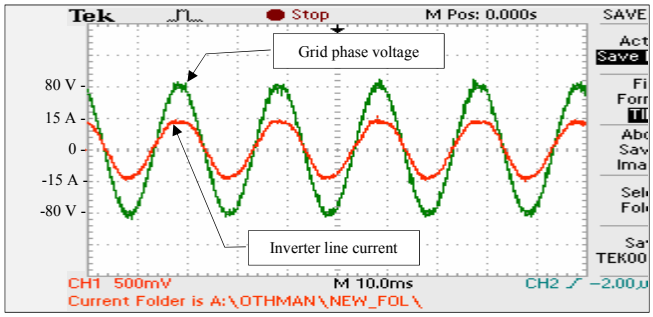

Fig. 7. grid voltage and inverter current in phase *a* (10 ms/div)

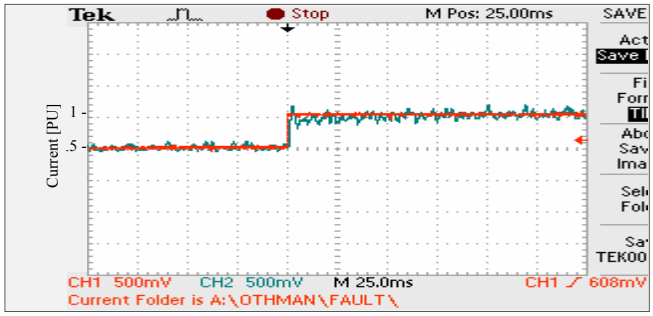

Fig. 8. Refrence current with inverter current step change (25 ms/div)

B. *Conditions of imbalance*

Fig. 10 shows the total inverter output phase voltages with 50% voltage drift in the DC-link of one cell in phase *a*. The change in the neutral point of the inverter can be clearly observed, because the inverter phase voltages appear to be unbalanced, whereas the inverter currents injected to the grid are staying almost balanced as illustrated in Fig. 11.

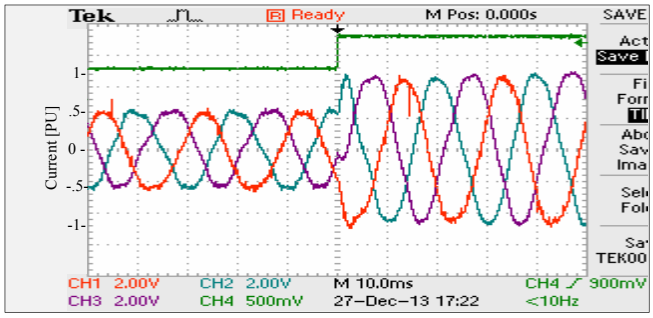

Fig. 9. Inverter current with 50% step change (10 ms/div)

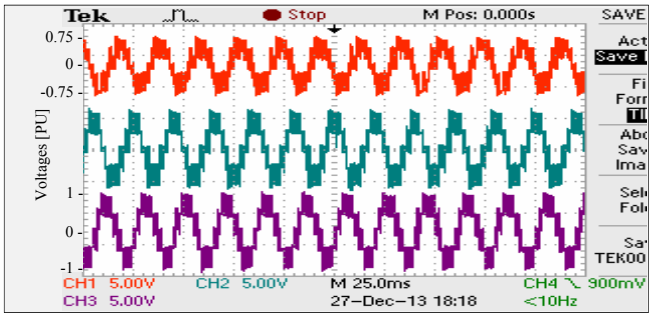

Fig. 10. Total inverter phase voltages with 50% DC-link voltage drift in one cell of phase *a* (25 ms/div)

Finally Fig. 12 shows the effectiveness of the modulation index feedforward compensation, where v_{ca}^{*} is the reference voltage of phase a before compensation and v_{ca}^{**} is the same reference after compensation.

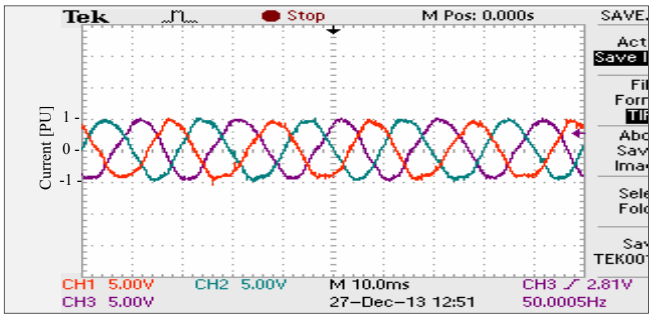

Fig. 11. Inverter currents with 50% DC-link voltage drift in one cell of phase *a* (with compensation) (10 ms/div)

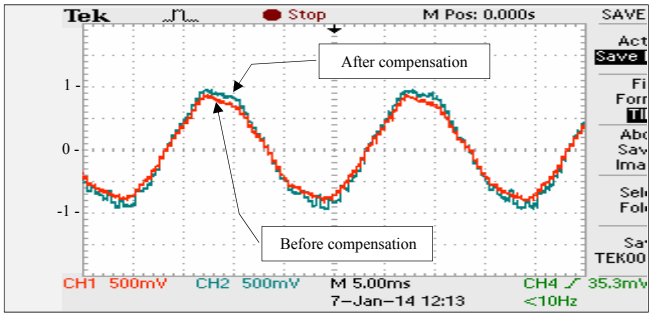

Fig. 12. Modulation index of phase *a* before and after compensation (5 ms/div)

V. CONCLUSION AND OUTLOOK

In this paper a three-phase 5-level cascaded H-bridge inverter topology has been proposed for the grid connection of power generation systems out of renewable energy sources. The grid connection process is controlled using a voltage oriented control technique. The system is designed in a flexible and versatile way for the investigation of different PV and hybrid schemes of energy generation. In the present paper the injection of a balanced system of currents with unity power factor to the grid is presented. A simple DC-link voltage feedforward compensation control is used to support the VOC-scheme in keeping balanced currents even if the inverter output phase voltages are unbalanced due to voltage

changes in the DC-links. The performance of the proposed controller and the overall grid-connected system are investigated based on a MATLAB/Simulink environment as well as on laboratory setup. A SV-PWM algorithm was used for generating the firing patterns for the IGBT-inverters. The VOC with a feedforward compensation as well as the SVPWM algorithm are implemented by using a TMS320F28335 DSP platform. The results show that the inverter maintains the injection of balanced currents to the grid with unity power factor even for a change in the DC-link of one H-bridge cell to 50% of the nominal value. In the same project the ongoing work is dedicated to the investigation of hybrid systems in which the DC-links are fed by PV-panels as well as by variable speed turbines.

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